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作品名稱
內建自我測試之三角積分式類比數位轉換器：適用於3D IC內建類比數位轉換器之整合型測試解決方案
A Built-in Self-Test Σ-Δ ADC: an Integrated Test Solution for the ADCs in 3D ICs

隊伍名稱
快很準 / Quick, Easy, and Accurate

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作品摘要

在莫爾定律即將走到盡頭的今日，半導體產業界相信3D IC將會是未來趨勢，像是through-silicon via（TSV）般的3D技術可提供電路間短距離垂直連接的機會，使電路效能有所突破並再創新高。IC測試技術因此面臨許多前所未見的挑戰，其中最大的瓶頸在於3D IC的I/O pad可能只存在於最上層和最下層晶片，位於內層晶片的電路缺乏與外部直接連接的I/O pad，因此傳統的測試技術無法直接應用在3D IC上。尤其是對於高效能混合訊號電路而言，不但要驗證其功能正確性，還要檢驗其效能是否符合設計規格，更是一道艱難的關卡。各專家學者紛紛對3D IC提出了測試策略，並一致認同易測試性設計（design-for-testability, DfT）及內建自我測試（built-in self-test, BIST）將是測試3D IC不可或缺的兩項關鍵技術。

本作品為3D IC提供一個ADC測試解決方案，實現了一個高精準度且達到全頻寬測試之全整合型BIST Σ-Δ ADC，本設計中同時實現了數位可測試性設計（decorrelating design-for-digital-testability, D^3T）及BIST電路設計兩項技術。在ADC設計中我們加入了D^3T結構，D^3T電路可將經Σ-Δ調變後的數位位元串流訊號轉換為測試所需的類比訊號，並保證所產生的測試訊號是絕對線性，且因D^3T結構重複使用原電路多數元件、只加入少數開關，因此具有高錯誤可觀測性、低硬體成本的優點，並可進行全速測試。

為降低BIST設計之硬體成本，我們提出了一個運算複雜度及硬體需求較低的嶄新in-phase and quadrature waves fitting （IQWF）演算法。IQWF演算法是在時域上對待測ADC的輸出響應進行同步且即時（real-time）的分析運算，因不像傳統FFT分析需儲存所有的ADC輸出，所以可大幅降低硬體成本。BIST可測得的參數包括SNDR、dynamic range、offset、gain error等，符合工業界標準測試需求，故相當適合BIST電路設計。此外，BIST電路是以全數位實現，使其達到高強健性、低面積、低功耗、易於移植到新製程等優點。

Fig.1為Σ-Δ ADC的測試結果，晶片的BIST量測結果顯示所測得之dynamic range 高達92.1dB、peak SNDR可達到87.4dB，與傳統類比測試使用FFT分析之測試結果非常接近。Fig.2為frequency response測試結果，BIST測試頻寬完全涵蓋待測ADC之額定20kHz音頻訊號頻寬，成功達成了低成本與高測試準確度的設計目標，更提供了3D IC一個完善的ADC測試解決方案。

Abstract

The 3D IC is considered as one of the emerging techniques for implementing the next-generation ICs. The 3D IC technique such as through-silicon vias (TSVs) provides vertical and shorter connections for inter-die communication. Hence, the 3D IC achieves many advantages such as increased functional density, decreased power, more compact volume, reduced signal latency, and higher performance. On the other hand, the 3D structure leads to new test challenges. The main issue of testing 3D ICs is the reduced controllability and observability due to the lack of accessible I/O pads. After packaging, the 3D ICs still need to perform the final tests; the I/O pads of the inter dies, however, may be no longer directly accessible during the final tests. New test strategies are requested to address the test challenges. From the testing points of view, the circuits under test (CUTs) incorporated with some on-chip design-for-testability (DfT) or built-in self-test (BIST) functions are highly demanded for 3D ICs.

This work provides an integrated test solution for the ADCs in 3D ICs. We implement a fully integrated BIST Σ-Δ ADC which achieves a high resolution and a BIST bandwidth as wide as the rated input bandwidth. We adopt the decorrelating design-for-digital-testability (D^3T) scheme to implement the input stage of the Σ-Δ ADC under test (AUT). The D^3T scheme accepts digital Σ-Δ modulated bit-streams and then generates the required analog stimuli. In addition, the D^3T structure also provides the advantages such as a small silicon overhead, high fault observability, and the capability of conducting at-speed tests.

We propose a novel in-phase and quadrature waves fitting (IQWF) method for implementing the BIST design with a low cost. The IQWF method conducts single-tone functional tests to provide the standard test results requested by industry such as the SNDR, the dynamic range, the offset, and the gain error of the AUT. Since the proposed IQWF procedure is performed digitally in real time, it does not require any analog design effort and huge memory like conventional Fast Fourier Transform (FFT) analysis does. The all-digital implementation of the IQWF method features robustness, low-power, a small area, and portability. These characteristics make the IQWF method well suitable for BIST implementations.

Fig. 1 depicts the dynamic range test results. The BIST circuits report a dynamic range of 92.1 dB and a peak SNDR of 87.6 dB, which are very close to the corresponding test results obtained by conventional FFT analysis. Fig. 2 shows the frequency response test results. The BIST circuits achieve a test bandwidth as wide as the AUT's 20-kHz rated input bandwidth. In conclusion, we successfully implemented the fully integrated BIST Σ-Δ ADC with a low cost and high test accuracy. It provides an integrated test solution for the ADCs in 3D ICs.

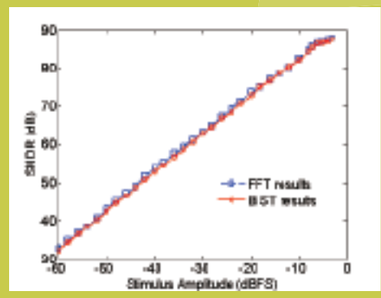

Fig.1 > Dynamic range test result

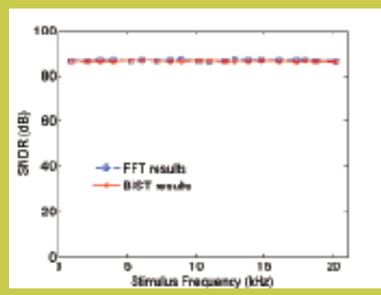

Fig.2 > Frequency response test results

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分別於1990年、1992年和2003年取得清華大學電機工程學系學士、碩士與博士學位。1997至2001年期間，任職於台灣積體電路製造股份有限公司，從事類比矽智財設計。2001年加入積丞科技，擔任類比矽智財部資深經理。2004年起，任職於交通大學電機工程學系迄今。

研究領域

混合訊號電路設計及其design-for-testability （DfT）、built-in self-test （BIST）、calibration等技術設計。