D12-014

作品名稱
臨界電壓晶片資料傳輸
Near-threshold On-chip Data Link

隊伍名稱
低到你無法想像 / Low as you want

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作品摘要

近年來，「環保綠能、永續生存」是近年來各界發展的重點。然而近臨界電路的設計將元件操作在近臨界區，目的是大幅降低功耗，達到所謂的效率能源（Energy-Efficient）的特色。但是它有幾個主要的瓶頸：第一、操作速度慢，多應用於生醫晶片或其它慢速的系統。第二、靜態漏電功率消耗的問題在近臨界區下更顯得嚴重。第三、嚴重的製程漂移，影響著良率與量產成本。

在本企劃書中，我們提出了臨界電壓系統單晶片（System on Chip, SoC）上的資料傳輸（Data Link）電路設計。並以局部升壓（Local Boosting)的）概念提出一系列全新的靴帶式技術（ootstrap Techniques），解決近臨界區電路設計的問題。我們提出的靴帶式技術，主要概念是使電路可提供雙向的升壓功能，所謂的雙向，是同時對P型跟N型元件作用，一邊大幅地增加驅動力，一邊抑制靜態漏電。相較於傳統電路操作在近臨界區，可以有兩個Order的改善。另一個的優點就是靴帶式技術可以使在次臨界區操作電壓下的電路，操作在一般的三極管區（Triode Region），使得電路模型更加精確。我們從電路的蒙地卡羅分析就可以清楚地了解到製程漂移因此大幅減少。

本設計的目標是完成臨界操作電壓下，可達40Mbps的傳輸，並達到高能源效率（Energy Efficiency）。我們一共呈現了兩個相關的電路：（1）一個應用在晶片匯流排（On-chip Bus）上，能有效抑制符號干擾（Inter-Symbol Interference, ISI）的靴帶式中繼器設計，V_{DD} = 0.3V時，單一個Channel最高可以傳輸100Mbps的資料傳輸率，即便在V_{DD} = 0.1V時，仍有0.8Mbps的資料傳輸率。（2）靴帶式振盪器（Bootstrapped Ring Oscillator），並完成了一個可操作在近臨界電壓的全數位鎖位迴路（All-digital PLL, ADPLL）。操作在0.25V時，這個ADPLL最高可提供44.8MHz輸出頻率，僅有消耗2.4μW的功率，而在0.5V時，可提供480MHz的輸出頻率，78μW的功率消耗。

Abstract

For the sustainable electronic devices, ultra-low power design is essential to prolong the battery lives. According to $P = fCV^2$, scaling the supply voltage down is the most effective way to reduce the power consumption. According to the forecast from the International Technology Roadmap for Semiconductors (ITRS), the supply voltage will be scaled to 0.5V for low-power applications within the next generation. Scaling the supply voltage near the threshold voltage is the most favorable solution for low-power designs. On the other hand, Nano-scaled devices exceed the limit of the speed in the near-threshold region based on small device loading. Nano-scaled process is broadly applied to ultra-low power designs, which includes RF, AD/DA, MPU, especially in biomedical applications. Emerging embedded biomedical applications have once more pushed the low-power designs into another extreme case.

In order to achieve the feature of the energy-efficient operation, the designs are applied to work using near-threshold supply. However, near-threshold circuit design is definitely challenging because the driving capability (Ion), which is limited to apply to slow system. Then, the static leakage power becomes severe, and decreases the Ion/Ioff ratio. Moreover, process variations are degraded significantly, affecting the circuit performance, the power efficiency, and the fabrication yield.

In this work, we have proposed an on-chip data link system at near-threshold supply using local boosting techniques. In order to improve the design issues in the near-threshold region, we have developed several bootstrapped circuits. The main contribution of the proposed bootstrapped techniques is to boost the gate voltage at the both sides, which means to boost the gate voltage of the PMOS and NMOS at the same time. The proposed circuit is applicable in both increasing driving ability by boosting signals into super-threshold region and reducing the leakage current. While the circuit is operated in sub-threshold region, two-order improvement is achieved. In addition, the bootstrapped circuits are operated in triode region with the near-threshold supply. Consequently, that explain why the process variation affects the proposed design scheme to a lesser extent. We can verify it with simulations of Monte Carlo analysis.

Two build blocks using bootstrapped circuits in on-chip data link have been proposed. The first one is an ISI-suppressed bootstrapped repeater applied to on-chip bus is proposed. The bootstrapped CMOS repeaters are inserted to drive a 10mm on-chip bus. Additionally, a precharge enhancement scheme increases the speed of the data transmission, and a leakage current reduction technique suppresses ISI jitter. The measured results demonstrate that for a 10-mm on-chip bus, it can achieve 100Mbps data rate at 0.3V, and even 0.8 Mbps at 0.1V. Then, we present a near-threshold supply ADPLL with bootstrapped digitally-controlled ring oscillator (BDCO) that allows an ADPLL to operate with a near-threshold supply. The BDCO is composed of a bootstrapped ring oscillator (BTRO) and a weighted thermometer-controlled resistance network (WTRN). The proposed bootstrapped delay cell generates large gate voltage swing to improve the driving capability significantly. The boosted output swing keeps the transistors operated in the linear region to provide high linearity of the output frequency as function of VDD even using a near-threshold supply. According to the transferring character of the BTRO, WTRN provides linear control while sweeping the supply voltage. The proposed ADPLL oscillates from 36.8 to 480MHz with a power consumption of 2.4-78μW under a supply voltage of 0.25-0.5V.

指導教授

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1990年取得美國威斯康辛大學電機電腦工程學系博士，1990~2002年任教於中央大學電機系教授，2002年迄今任交通大學電控系教授。另擔任經濟部技審會技審委員；經濟部技術處SBIR審查委員、SBIR電子領域召集委員以及教育部顧問室顧問等。

研究領域

混合信號電路設計與測試、高速資料鏈結、低電壓低功率晶片設計、生醫類比前端電路以及車用電子設計等。