D12-003

作品名稱	8x8 多天線晶格簡化偵測器晶片 8x8 Lattice Reduction Aided MIMO Detector Chip
隊伍名稱	亮晶晶格隊 / Shining lattice team
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作品摘要 Abstract

高維度多輸入天線對多輸出天線系統（MIMO）已逐漸為當今無線通訊系統的主流。MIMO 傳輸具有二大優點，第一為可增加資料傳輸速率及頻帶使用率，第二為增加通道的多樣性，可用來降低環境通道衰減所造成的影響。因此多輸入多輸出解碼器的主題被廣泛討論及應用，本研究之目的在於設計出支援多輸入多輸出解碼器之晶格簡化偵測器的整體架構。現有的文獻已提出了 FPGA 的實作架構跟之前提出在 4 根天線下的 VLSI 實做，但是關於晶格簡化演算法前的 QR 分解與之後的偵測器設計則上沒有任何文獻。且目前文獻上都著眼在 4 根天線，本人預計使用改良過的固定吞吐量的晶格簡化演算法結合吉文思旋轉的 QR 分解演算法，設計出一個完整的 MIMO 前置電路，並利用元件共用減少硬體支出，此外後方預計使用改良的低延遲 K-Best 多輸入多輸出解碼器來完成，整個系統實做更是上看到 8 根天線，預計在這個領域算是相當領先的作品，並驗證在高維度天線的無線通訊系統下，依舊能提供一個低硬體複雜度跟高效能 BER（bit error rate）的解決方法。

High dimensional MIMO systems gradually become the main technique to use in wireless communication system. It has two advantages, one is increasing the data rate and spectral efficiency, and the other is to improve the detection performance using diversity. This study propose to fulfill a lattice reduction aided MIMO detection in 8 by 8 MIMO system. Although the previous thesis proposed several lattice reduction (LR) processors. The QR decomposition before LR and detectors after LR are all neglected. And the dimension mentioned is all below 4 antennas. So we proposed a preprocessing structures which shares the common Givens rotation processors and hardware to do QR decomposition and LR algorithm. And then a sorting-reduced K-best detector is proposed to achieve short latency with low complexity. And the total system is proposed to use under 8 by 8 MIMO systems. We believed this work have lots contribution to this criterion. And this work also verifies that MIMO detection with acceptable complexity can still achieve high performance (low bit error rate).