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作品名稱	可彈性多層堆疊之三維記憶體設計 3D memory design with flexible multi-layer stacking
隊伍名稱	超級咩摩瑞 / SUPER memory
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作品摘要 Abstract

隨著製程為了繼續遵循莫爾定律不斷演進，三維製程整合是目前最有潛力能突破莫爾定律並有效提升效能及密度的方法。目前三維製程的開發正在萌芽階段，但有許多問題已經開始浮現。

我們提出了半主從式堆疊架構以及自我時序追蹤差動傳輸方案。半主從式結構為一種堆疊的架構，主要是將堆疊的晶片分為主層跟僕層，主層只有一個，僕層具有堆疊的延展性，由於時脈是由僕層自我產生，半主從式結構有著良好的堆疊特性以及良率。

自我時序追蹤差動傳輸方案包含了差動小訊號及自我時序追蹤。差動小訊號方案能夠有效提高直通矽穿孔 (TSV) 下的傳輸效率，而自我時序追蹤則可以在不同層數堆疊的情形下精準的控制操作時序，也因此可以同時支援任意層數的堆疊及適應直通矽穿孔的製程變異。

我們的電路由三萬兩千字元之靜態隨機存取記憶體所組成，量測結果顯示在我們的架構能夠適應至少二十層的堆疊，此電路也是第一個由台灣成功生產之三維堆疊晶片。

We have to face a lot of technical difficulties and physical limitations as process follows Moore’ s Law continuously. 3D integration has the most potential to solve these problems and provide outstanding performance and high density. We design a Semi-Master-Slave scheme and Self-Timed Differential-TSV Signal Transfer Scheme in this project.

A Semi-Master-Slave scheme solves the stacking conditions such like yield, at-speed testing, and die-to-die variation. Semi-Master Slave scheme has a master-layer and slave-layers. Master-layer controls the logic signal and sends to slave-layer. Each slave-layer generates its own pulse signal. Finally, master-layer receives data from slave-layer. Compare to Direct-Stack and Traditional Master-slave, our Semi-Master-Slave is a better way for 3D IC stacking. MS structure faces low yield and cannot perform at-speed testing for each slave die. These problems are solved in our Semi-Master-Slave scheme.

Self-Timed Differential-TSV Signal Transfer Scheme reduces the speed penalty of TSV and support the multi-layer stacking function, and the effect of TSV process variation can be reduced also.

This circuit can support most of the memory stack (DRAM, SRAM, etc), and this circuit has better energy saving capabilities in wide I/Os. A 32kb 2 layer 3D-SRAM macro has been fabricated and it is the first fabricated TSV-based 3D-SRAM in Taiwan and the demonstrated stacking layer scalable 3D-SRAM in the world for the first time.