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作品名稱	應用於隨機存取記憶體之透明式線上自我修復技術 **Transparent Online Built-In Self-Repair Scheme for RAMs**
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作品摘要 Abstract

在系統晶片中內嵌式記憶體一般佔有相當大之面積，而且記憶體通常使用侵略性設計準則做設計，造成記憶體易有良率與可靠性不佳之問題，因此改善記憶體的良率與可靠度對於系統晶片來說絕對必要的。其中錯誤更正碼與自我修復技術已經廣泛用於改善內嵌式記憶體的良率與可靠性。此競賽作品，我們提出一用於具有 ECC 記憶體之透明式線上自我修復技術。在生產階段，此技術可以執行測試與修復功能以達到增進記憶體良率之目的。在使用階段，此技術可以執行週期性透明測試且利用在製造階段沒用完之備份元件修復在使用過程中壞掉之元件，達到改善記憶體可靠性之目的。實驗結果顯示，所提透明式測試線上自我修復技術可大幅提升系統的可靠度，而且對於一個 8Kx72 的記憶體僅需要付出約 2.4% 的硬體成本。

Embedded memories usually occupy a significant portion of the chip area in modern system-on-chip (SOC) designs. Memories are designed with the smallest transistors and aggressive design rules, such that they are prone to the problems of yield and reliability. Thus, improving the yield and reliability of memory cores is very imperative for SOC designs. Error correction code (ECC) and built-in self-repair (BISR) techniques have been considered as good approaches for enhancing the reliability and yield of embedded memories. In this contest, a transparent online BISR scheme for RAMs with ECC is proposed. The transparent online BISR can perform off-line test/repair for RAMs in production phase. This can enhance the yield of RAMs. It also can perform online test/repair for RAMs in life time. In online test/repair mode, the transparent online BISR scheme performs transparent march tests for the RAM under test and repairs the RAM cells with hard faults if there are remained redundancies after the off-line test/repair phase. This can improve the reliability of RAMs. Experimental results show that the area cost of the proposed transparent online BISR scheme for RAMs with ECC is low—only about 2.4% for an 8K×72-bit SRAM.