0.22V 2MHz Ultra-Low Voltage and High-Performance Read-Only Memory

0.22V 2MHz 超低電壓高速唯讀記憶體設計

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作品摘要 Abstract

本作品提出了一套低電壓高速ROM的位元陣列架構以及具PVT變異容忍度的周邊電路設計。位元陣列架構包含三種技術:一、使用源極編碼ROM細胞元,徹底解決資料編碼衍伸出的輕重載問題;二,設計動態區段保護架構,以不需過多額外電路或增加編碼複雜度的條件下,解決串音導致讀「1」錯誤問題;三、階層化位元線,可縮小漏電流與減少漏電路徑提升On/Off電流比例,並降低位元線寄生電容以降低功率消耗與提昇讀取速度。此外,針對PVT Variation加入自我補償與感測機制之周邊電路設計,使得ROM能達到100%的編碼涵蓋率,更可於低電壓環境下擁有較佳操作速度。

最後,與ISSCC會議論文中低電壓ROM作品相比,於相同操作電壓(0.29V)下可達到4.76倍的效能提升,而在相同頻率操作下可更操作於更低電壓(0.22V)並達到58%的功率改善與較佳的功率效益。甚至它也滿足近年來ISSCC發表的幾項低電壓處理器的規格,間接引證了本作品可提供低功率與高效能嵌入式系統的絕佳解決方案。

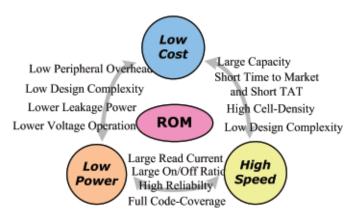


圖1>唯讀記憶體設計主要考量與設計趨勢

This work proposes the cell array architecture and PVT variation-tolerant peripherals for a low-voltage and high-speed ROM. The proposed cell array architecture contains three techniques: 1. Source Programming ROM-Cell, which overcame the data-dependent bitline loading problem; 2. Dynamic Segmentation Shielding Structure, which solves failure of reading "1" caused by crosstalk without additional circuits and encoding complexity; 3. Hierarchical Bitline, which not only narrows down leakage and paths to rise On/Off current ratio, but also reduces the parasitic capacitance of bitlines and supports higher-speed accesses. Moreover, the peripheral designs of self-compensation and sensing scheme tolerates PVT variation, making ROM reach 100% code-coverage, and contributes to better operating speed in low voltage environment.

Finally, compared to most ISSCC papers on low voltage ROM, our design gains 4.76X performance improvement at 0.29V, furthermore, it reduces 58% energy consumption to reach better power efficiency at lower 0.22V. The fact that this design meets the specifications of some low-voltage processors in recent ISSCC papers has proven indirectly that this work offers the best strategy for low-power and high-performance embedded systems.

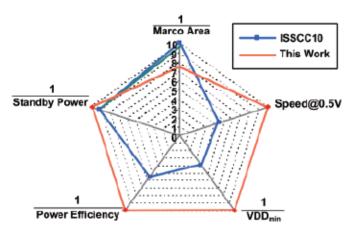


圖2>本作品與過去文獻之比較