D16-070
Design Group

電容電流偵測器校正與負載暫態響應最佳化技術及其實現於四相降壓轉換器

Capacitor-Current-Sensor Calibration and Load-Transient Optimization Techniques Implemented in a Four-Phase Buck Converter

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作品摘要

下世代處理器的電源管理單元，將面臨更大更快的負載電流變動，故需要非常快的反應速度；電源管理單元內的輸出電容電流可即時反映負載電流變動，可藉此控制以達負載暫態響應最佳化，即輸出電壓 Undershoot、Overshoot 與回復時間降到理論最小值，但偵測器準確度受輸出電容電流路徑的阻抗變異影響。

為達負載暫態響應最佳化，本作品提出二項技術。第一為電容電流偵測器校正技術，在輸出電容路徑的阻抗變異時，仍可偵測到準確的輸出電容電流；第二為暫態響應最佳化電路，根據準確的輸出電容電流資訊，準確地控制負載電流變動時的電感充放電時間。

本作品以 0.18μm 1.8V CMOS 製程實現一個四相降壓轉換器，晶片面積 1.93mm^2。量測結果顯示：當負載電流由 0.2A 變動為 2A 時，輸出電壓 Undershoot 由 225mV 降低至 100mV，回復時間由 712ns 縮短為 133ns；當負載電流由 2A 變動為 0.2A 時，輸出電壓 Overshoot 為 81mV，回復時間由 370ns 縮短為 113ns。本作品輸出電壓 Undershoot 與其理論最小值的比例與現有最佳文獻差不多，回復時間與其理論最小值的比例遠勝現有最佳文獻。

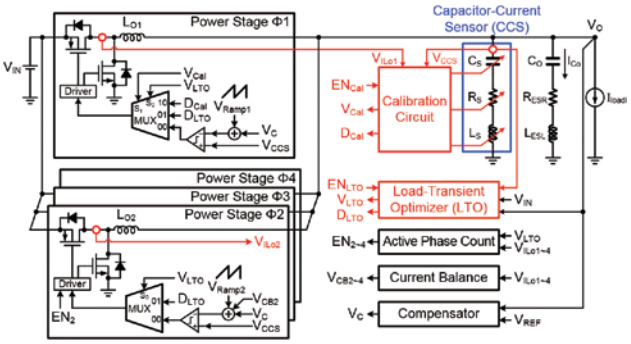

Fig 1. System architecture

Abstract

Power management units (PMUs) for the next-generation processors need an ultra-fast response because of the encountered large and rapid load current changings. In PMUs, the output capacitor current I_{Co} can instantly reflect the changings of load current, and load-transient optimization can be achieved by an I_{Co}-based control. The load-transient optimization means the output voltage's undershoot ΔV_{US}, overshoot ΔV_{OS}, and settling time t_S are reduced to the theoretical minima. However, the accuracy of the I_{Co} sensor are affected by the impedance variations in the I_{Co} path.

To achieve load-transient optimization, this work proposes two techniques. The first is capacitor-current-sensor calibration technique, by which accurately-sensed I_{Co} can be obtained under the impedance variations in the I_{Co} path. The second is load-transient optimization circuit, by which the charging and discharging times of the output inductor can be accurately controlled based on the accurately-sensed I_{Co}.

This work implements a four-phase buck converter with the proposed techniques in a 0.18μm 1.8V CMOS process, and the chip area is 1.93mm^2. Measurement results show that for a 0.2A-to-2A load-current step, with the proposed techniques, ΔV_{US} and t_S are respectively reduced from 225mV and 712ns to 100mV and 133ns. In contrast, for a 2A-to-0.2A load-current step, ΔV_{OS} is 81mW, and t_S is reduced from 370ns to 113ns. In this work, the ratio of ΔV_{US} to its theoretical minimum is comparable with the best of state-of-the-art works, while the ratio of t_S to its theoretical minimum greatly outperforms the best of state-of-the-art works.