Design Group
D17-006

一個免矯正之全類比式十二位元每秒取樣五千萬次連續漸進式類比數位轉換器

A Calibration Free 12-bit 50 MS/s Full-Analog SAR ADC

隊伍名稱 混訊天王
God of Mixed-Signal

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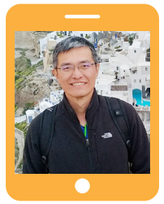

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研究領域

CMOS 影像偵測 IC 設計、低壓低功耗類比數位轉換器設計、類比前級電路設計、智慧型影像應用單晶片設計、生醫應用影像感測 IC 設計、類比與混波 IC 設計。

作品摘要

近年來，受益於先進製程的微縮效益，尖端科技的連續漸進逼近式類比數位轉換器（SAR ADC）已經達到了 12-14 bit 與 10-100 MS/s 的規格。然而，以 40 nm 作為分界點，相較於落後的製程，單通道的 SAR ADC 成長速度已漸趨於緩，此趨緩原因可大致歸因於兩大面向，其一為所有先進製程所有的共同缺點：寄生效應比重增加，因製程微縮使得導線間、元件間甚至 MOS 節點間的距離縮小，造成寄生電容比重上升，尤其當 ADC 的解析度及速度的提升，其影響更趨於嚴重。因此，電路限制不再受限於元件特性而是寄生效應，也使得在 pre-layout 及 post-layout 的結果有很大的出入，大幅增加設計難度。另一為傳統 SAR ADC 的進步主要受益於製程微縮，其大大地增加數位電路的操作速度及被動元件的準確度。相對地，除了寄生效應外，隨著解析度及操作速度的提升，類比電路的規格需求卻變得過於嚴苛。因此，高速高解析度 ADC 的設計中，上述兩個面向變成了最急迫、最困難且最需要被解決舒緩的問題。

雖有上述限制，提升 SAR ADC 規格的最直覺的方法為使用時間交錯式（TI）以及一次比較多位元（M-bit/cycle）或是同時使用此兩種方法以繞過其限制，但是，除了轉換效率較差及電路複雜度較高之外，為了解決架構附帶的非理想效應如偏移誤差、增益誤差以及通道誤差…等等，使用前景或是背景矯正電路機制是必要的。不幸地，就算使用了矯正機制，其解析度瓶頸依舊存在，因此，我們專注於提升單通道 SAR ADC 的規格且使用單一位元轉換（1-bit/cycle）伴隨著最高效率的類比數位轉換效率、最低的電路複雜度及無須任何額外的矯正電路機制。

在傳統 SAR ADC 中，SAR logic 消耗了很大比重的功耗且占據了大部分的 SAR 迴圈延遲，且僅有控制功能，對於 ADC 的規格並沒有實質上的貢獻。然而，因為數位電路尺寸的大幅縮小且寄生效應比重大幅上升，其大幅地惡化了 SAR logic 的操作速度及其功耗。直覺地，省去 SAR logic 且依舊能達到 SAR 的轉換應是一個最好且最理想的方法以提升整體 ADC 規格。

在本設計中，我們提出了一個全類比式的 SAR ADC 以完整運用位元轉換週期的時間及功耗分配，省略所有 SAR logic 且不受寄生效應影響以降低所有類比電路的規格需求。此外，相較於傳統離散時間操作，全類比式架構使用連續時間操作以降低準位電壓產生器的規格需求。最重要的是，本設計不需任何矯正機制，所有的非理想效應如電壓偏移、亞穩態及雜訊皆可被減緩甚至消除。

本設計提出一個 12-bit 50 MS/s SAR ADC，其使用全類比式架構以突破在先進製程中的限制，操作於 0.9 V，僅消耗 0.34 mW，在 Nyquist 取樣率，達到 64.1 dB SNDR 及 75.6 dB SFDR，5.3 fJ/conv.-step Walden FoMW 及 172.8 dB Schreier FoMS。此 ADC 使用 1P9M 40 nm CMOS 製作，總面積僅 0.01 mm^2。

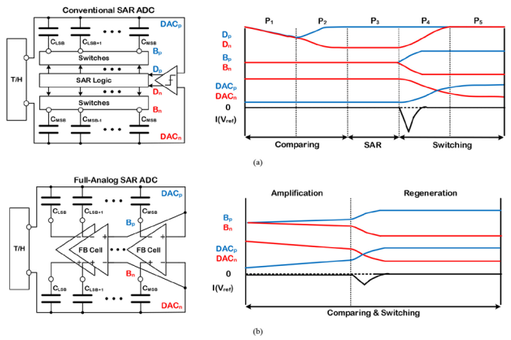

圖 1. 架構與操作比較：（a）傳統連續漸進是類比數位轉換器與（b）全類比式連續漸進式類比數位轉換器

Abstract

In recent years, the state-of-the-art SAR ADCs have achieved 12-14 bit and 10-100 MS/s due to the scaling of advanced CMOS technology. However, compared to the process nodes behind 40 nm CMOS, the improvement of single-channel SAR ADC has slowed down at the process nodes beyond 40 nm CMOS. The slowdown of ADC improvement is attributed to two main aspects. One aspect is the common drawback at the advanced process nodes, the parasitic capacitances due to the shrinking spacing among wires, devices, and even MOS terminals, where the parasitic have occupied considerable proportion as the ADC resolution and bandwidth increase. Thus, the design limitations are no longer dominated by the MOS intrinsic characteristics but the parasitic effect, which increases the difficulty in designing with the consistent outcomes between pre-layout and post-layout simulations. The other aspect is that the improvement of SAR ADCs is mainly benefited from the device scaling of digital circuits （SAR logic）and the accuracy of passive device（DAC）, in contrast, the requirements of analog circuits （T/H, comparator, and DAC switches） become relatively rigorous with the increasing ADC resolution and bandwidth. Hence, the parasitic effect and rigorous analog requirement become the most tough issues to be solved or relaxed particularly in high speed and high resolution SAR ADCs.

Recently, despite the aforementioned limitations, the popular approaches to improve SAR ADC performance are to bypass the limitations by performing analog-to-digital （A-to-D） conversion in the architectures of time-interleaved （TI）, multi-bit per cycle （M-bit/cycle）, or in conjunction with both techniques, which are the relatively intuitive solutions to push the ADC specifications. However, in addition to the drawbacks of inefficiency and the cost of complexity have been introduced, the calibration in foreground or background is inevitable due to the collateral non-ideal effects （offset mismatch, gain mismatch, channel mismatch, and so on） in both architectures. Unfortunately, both architectures of TI and M-bit/cycle have the resolution limitation even though the calibration is applied. Thus, in this work, we aim at improving the performance of single-channel SAR ADC with single bit per cycle（1-bit/cycle） with the most efficient A-to-D conversion, the lowest complexity, and no additional calibration.

In the conventional SAR ADCs, SAR logic consumes a large proportion of power dissipation and occupies the most part of SAR loop delay. Worst of all, SAR logic contributes nothing to the ADC performance since it only acts as a function-level block. Moreover, the parasitic effect deteriorates the speed and power dissipation of SAR logic the most since the dimensions of digital circuit are scaled and the parasitic of wire load dominates the nodal capacitance. Intuitively, to eliminate SAR logic without failing to do SAR operation becomes the best and ideal solution to improve the ADC performance.

In this work, we propose a full-analog SAR ADC to fully utilize the timing and power budgets in a bit-cycling conversion and relax the requirements of analog circuits by eliminating SAR logic entirely without the influence of the degradation from parasitic effect. Besides, compared to the conventional discrete-time （DT） operation within a bit-cycling conversion, the proposed ADC operates in continuous-time （CT） which highly relaxes the requirements of reference generator. Most of all, the proposed full-analog SAR ADC is implemented without any calibration, where the non-ideal effects （offset, meta-stability, and noise） are mitigated and eliminated.

This work presents a 12-bit 50 MS/s SAR ADC in full-analog architecture to overcome the limitations at the advanced process node. With a 0.9V supply voltage, the prototype SAR ADC consumes a total power of 0.34 mW. At Nyquist rate, the ADC achieves a signal-to-noise-and-distortion ratio （SNDR） of 64.1 dB, a spurious free dynamic range （SFDR） of 74.4 dB, and a resulting Walden figures of merit （FoMW） of 5.3 fJ/conversion-step and Schreier figures of merit （FoMS） of 172.8 dB. The ADC core fabricated in 1P9M 40 nm CMOS technology occupies an active area of 0.01 mm^2.