Design Group
D17-024

利用非同步取樣的低功率消耗與高解析度抖動偵測器

A Low-Power and High-Resolution Jitter Detector Using Asynchronous Sampling

隊伍名稱　滿滿的大平台
Fully Jumbo Platform
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研究領域
類比 / 數位積體電路、鎖相迴路及延遲鎖定迴路、通信積體電路、混合式及射頻積體電路系統、 微感測器積體電路、 類比數位轉換器。

作品摘要

現今，隨著半導體製程往摩爾定律方向持續前進，電路設計的技術日新月異，對於有線資料傳輸速度的要求也愈來愈高，目前已可達到數十個 Gbps。然而，高速傳輸卻受限於通道的不理想性造成資料的劣化，通常以加入等化器和時脈資料回復電路（Clock/Data Recovery Circuit，CDR）來緩解資料傳輸時的不理想效應。其中等化器是用來減少時域上的符際干擾（Inter-symbol Interference，ISI），以降低接收端資料的誤碼率（Bit Error Rate，BER）；另外，時脈資料回復電路則可從較大抖動的資料中萃取出一同步時脈，並對輸入資料重新取樣（Retime），可有效降低資料的抖動情形。對於時脈資料回復電路來說，抖動的轉移函數（Jitter Transfer）、容忍度（Jitter Tolerance）與生成（Jitter Generation）等參數，通常被用來評估此電路的特性。換句話說，抖動對於電路設計而言為一個非常重要的考量。就量測手法而言，傳統上量測資料抖動需要昂貴的自動量測儀器（Automatic Test Equipment）與晶片內的寬頻緩衝器（Buffer）。為解決上述的不便，本研究提出以單晶片系統電路的方式，在晶片內部偵測資料抖動的分佈，並達到更低功率消耗及更高偵測解析度的目標。其中，由圖一可見有線通訊系統與抖動偵測器的關係。

本研究提出一個有別於傳統的資料抖動偵測的技術，採低速、多相位、非同步取樣的方式，並驗證於 2.5Gbps 具隨機與週期性抖動的串列資料。此抖動偵測技術具備四項優勢：其一，可以低速延遲鎖定迴路產生取樣用之時脈，不需憑藉同步高速的時脈信號與任何倍頻迴路，除可避免穩定度的議題外，亦可達到小面積及低功率消耗的目的。其二，以多相位時脈取樣的方式，可增加偵測抖動時的時間解析度。其三，此提出的偵測技術可得到準確低失真的抖動參數絕對值，有別於過去僅可得到抖動大小的相對關係。最後，直接以此單晶片系統電路進行偵測，可排除昂貴的量測儀器和所需的寬頻緩衝器，同時可避免晶片與儀器間的各種變異干擾，大幅降低測量的成本。總結而言，此作品在晶片面積、功率消耗與精準度的折衷議題之間，提供了一嶄新的解決方法。

此偵測器實現於40奈米低功耗CMOS製程，操作電壓為1.1伏特，整體功率消耗僅 2.55 毫瓦，其中，延遲鎖定迴路消耗 2.25 毫瓦，取樣器與數位控制器等消耗 0.3 毫瓦。此系統的時間解析度可達到（1/19）資料位元，優於先前技術 2 倍以上，功率消耗與晶片面積也遠小於參考文獻。實驗結果顯示，對於現階段有線通訊系統而言，此偵測器具備實現上的可行性和其他成本優勢。最後，晶片的量測環境如圖二所示。

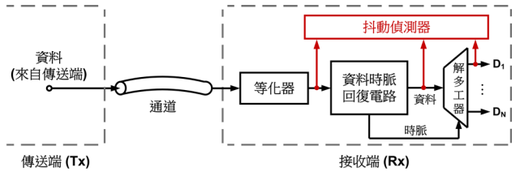

圖 1. 有線通訊系統與抖動偵測器

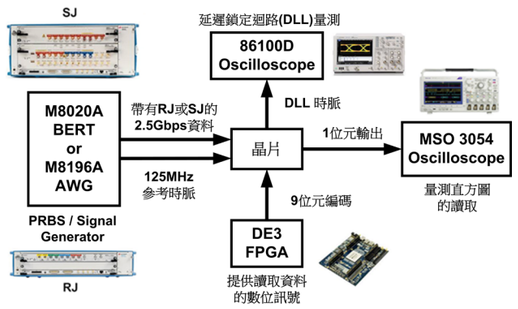

圖 2. 晶片的量測環境

Abstract

An equalizer and a clock/data recovery （CDR） circuit are the important building blocks in wireline communication systems. A nonlinear channel induces a severe inter-symbol interference （ISI）. By enhancing the high-frequency gain, the equalizer reduces the ISI and improves the jitter performance of the received data. The CDR circuit recovers the clock from the noisy data to generate the re-timed data. The jitter transfer function, jitter tolerance, and jitter generation usually characterize the performances of the CDR circuit. Therefore, the jitter is one of the key factors to characterize the equalizers and the CDR circuits. Generally, the automatic test equipment （ATE） and the high-speed I/O buffers are required to measure those above-mentioned circuits. However, the ATE is expensive and the high-speed I/O buffers are power hungry and sensitive to the noises. To overcome these disadvantages, an on-chip detector is attractive to measure the data jitter for an equalizer or a CDR circuit.

In this work, a jitter detector employing the low-power-consumption and high-resolution method is presented. The on-chip measurement using the low-speed, multi-phase, and asynchronous sampling clocks could construct a jitter histogram in which the discrete jitter distribution of the high-speed digital data can be obtained. For instance, a timing space of 20UI/19 between two adjacent sampling clocks is slightly larger than a UI. When the data jitter is small, the number of the data transitions might be 0, 1, or 2 within one timing space. By only recording the number of the twice data transitions, the histogram is generated to represent the discrete data jitter distribution. To generate the low-speed multi-phase sampling clocks, a delay-locked loop （DLL） is used instead of the PLL. The DLL uses a small capacitor as the loop filter and has no stability issue.

Fabricated in 40-nm CMOS technology, this detector totally consumes 2.55mW from a 1.1V supply, of which 2.25mW by the DLL, 0.30mW by the other digital logics. With 2.5Gbps PRBS-7 and 125MHz sampling clock sources, the proposed histogram can measure the rms Gaussian data jitter from 0 to 0.1UI with the maximum error 0.012UI. This histogram can also measure the peak-to-peak sinusoidal data jitter from 0 to 0.8UI with the maximum error 0.142UI. Finally, the resolution of this work is increased to UI/19 which is also at least two times smaller than prior references. Furthermore, the power consumption and area are less than before. Above all, this detector has remarkable potential for the feasibility of implementation and the cost advantage.

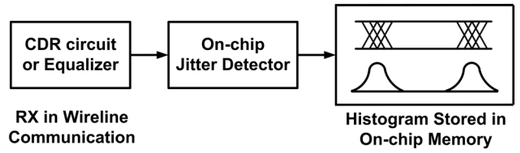

Fig 3. On-chip Jitter Detector and Measured Jitter Histogram