Design Group
D17-028

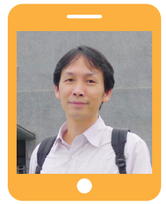
利用截波壓控震盪器達成面積高效之感測器介面電路

An Area-Efficient Chopper VCO-based Sensor Interface Circuit

隊伍名稱　震盪人生
Oscillating Life

隊　　長　涂智展 / 臺灣大學電子工程學研究所
隊　　員　王鈺凱 / 臺灣大學電子工程學研究所
陳翰群 / 臺灣大學電子工程學研究所

指導教授
林宗賢
臺灣大學電機工程學系



美國加州大學洛杉磯校區（UCLA）博士，現為臺灣大學電機工程學系教授。曾任職於博通（Broadcom Corporation）參與類比 / 射頻 / 混合訊號電路設計，並開發無線傳輸系統。

研究領域
生醫應用高能量效率無線通訊晶片、電源管理晶片、應用於 PLL 與 Delta-Sigma ADC 之混合信號電路設計技術、感測器與生醫應用類比訊號處理電路。

作品摘要

感測器將生活中的物理訊號，如溫度、磁場、生理訊號，轉換成人眼可讀的數位訊號。生活中的物理訊號，經過感測元件轉換成電壓或電流之後，需要經過感測器介面電路將訊號變成數位訊號。這些訊號的特徵，是非常微小，需要微伏特的解析度，以及主要落於低於一千赫茲的低頻。

傳統感測器介面電路的做法，是分別設計高性能的前端放大器將訊號放大之後，再設計高解析度的類比數位轉換器。為了簡化硬體架構，人們開始考慮直接使用一個高性能的類比數位轉換器，省略前端放大器的設計。這樣的設計，節省了硬體，但是卻提高了難度。在既有的文獻中，使用電壓為訊號處理基礎的做法，付出了相當大電路面積的代價。

近幾年，利用壓控震盪器，將電壓訊號變化轉換為時間與相位變化的做法漸漸流行。由於直流增益無限大的特性，讓此架構不須堆疊電晶體，適合低電壓操作；同時訊號處理使用大量數位電路取代類比電路，更適合整合入先進製程，符合未來物聯網的趨勢。然而，既有的文獻中，在感測器應用上，基於本方法設計之架構始終無法達到匹配於傳統做法之性能。

本作品模仿轉導電容連續時間三角積分類比數位轉換器的架構，設計出以壓控震盪器為基底，不需前端放大器，能直接應用於感測器的類比數位轉換器。其特色有三：

第一，壓控震盪器取代轉導電容積分器的設計，利用「電壓有限，相位無限」的特點，能夠大幅減少電路面積。

第二，利用壓控震盪器與轉導電容積分器相似的特性，加入截波技術，可以有效抑制低頻雜訊。

第三，仿照電容迴授儀表放大器的架構設計迴授網路，同時達到高阻抗、高線性度、高共模輸入範圍，且比起傳統的電流回授儀表放大器，擁有更低的功耗雜訊比。

本晶片使用 40 nm 製程實現，總共消耗 21 μW，在 ±50 mV 的輸入與 2 kHz 的頻寬中能達到 74.9 dB 的 SNDR 與 -82 dB 的 THD，面積為 0.06 mm^2。與傳統架構相比，本架構的面積縮小了 100 倍；而與其他壓控震盪器的架構相比，我們達到最好的 FoM。本作品亦實際放在磁感測器的應用下成功獨取正確之磁場訊號。

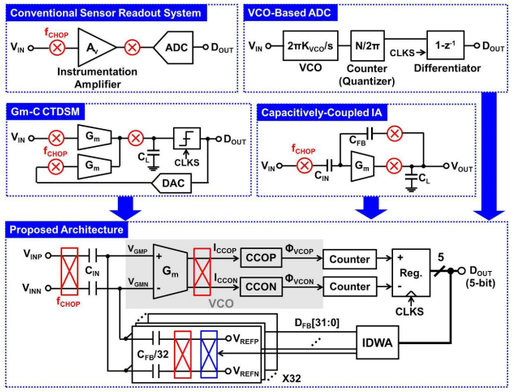


圖 1. 系統架構圖

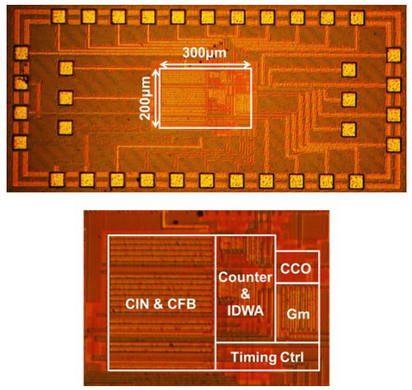


圖 2. 晶片圖

Abstract

Sensors convert physical signals in daily life into readable data, such like temperature, magnetic field, or bio-medical signals. The physical signals are transferred into voltage or current form by transducers, and the sensor interface circuits convert them to digital codes. The signals are very small with the resolution requirement of microvolts, and occupies small bandwidth from DC to several kHz.

The conventional implementation of sensor readout circuits separates the design into low-noise instrumentation amplifier （IA） and high-resolution analog-to-digital converter （ADC）. However, the design is usually complex accompanied with high cost. To save the hardware, it is possible to merge the IA and ADC together. However in the state-of-the-art, the approach with a Gm-C continuous-time delta-sigma modulator （CTDSM） without a IA sacrifices large circuit area to achieve the targeted resolution and accuracy.

Recently, voltage-controlled oscillators （VCO） are used to implement sensor interface circuits. The input voltage is converted to time-domain or phase-domain signal instead of voltage. It features infinite DC gain so that stacking transistors are no longer needed, and is suitable for low voltage operation in advanced processes. Furthermore, the signal processing circuits are highly digital, which makes them suitable to be integrated to advanced processes. However, the state-of-the-art works hardly achieve similar performances compared to conventional approaches.

In this work, a VCO-based ADC for sensors without preceding IA is proposed, which references the design principle of Gm-C CTDSM. The three features of this work are described below. First, the loop filter is implemented with VCO-based integrator instead of Gm-C integrator. Since the phase signal is limitless unlike the voltage signal is limited by supply voltage, large capacitor could be saved in the proposed design.

Second, by exploring the similarity of VCO-based integrator and Gm-C integrator, chopper could be added to mitigate the flicker noise problem.

Third, the feedback network similar to Capactively-Coupled IA provides high input impedance, linearity and input common-mode range. Compared to Current-Feedback IA, the proposed design achieves better power-noise efficiency.

The proposed work is implemented in 40 nm process, and the total power consumption is 21 μW. With ± 50mV input and 2 kHz BW, the measured SNDR is 74.9 dB and the THD is -82 dB. The circuit area is 0.06 mm2. Compared to conventional works, we achieved similar performance with 100X area reduction. While compared to state-of-the-art VCO-based approach, we achieved the best FoM. The function of the chip is further proved in the magnetic field sensing applications.

	This Work	JSSC 2012	ESSCIRC 2012	JSSC 2015	JSSC 2017	JSSC 2015	JSSC 2017
Typology	VCO-ADC (Close)	CFIA+ DTDSM	Gm-C CTDSM	Amp+ VCO-ADC	VCO-ADC (Open)	VCO-ADC (Close)	Time Domain
Tech	40nm	700nm	700nm	65nm	40nm	180nm	40nm
VDD	1.2V	5V	5V	0.5V	1.2V	1.8V	0.6V
Power	21μW	1.35mW	1.2mW	2.3μW	7μW	340μW	3.3μW
FSR	100mV$_{pp}$	80mV$_{pp}$	80mV$_{pp}$	1mV$_{pp}$	100mV$_{pp}$	4μA$_{DC}$	40mV$_{pp}$
BW	2kHz	10Hz	2kHz	500Hz	200Hz	1.25Hz	150Hz
f_{SAMPLE}	1MHz	10kHz	5MHz	1kHz	3kHz	10MHz	25MHz
SNDR	74.9dB	126dB*	90dB**	48.7dB	74dB	73dB	40dB
THD (f_{in})	**-82dB** (220Hz)	6ppm (INL)	-102dB (10Hz)	-52dB (10Hz)	-79dB (203Hz)	--	-40dB (11Hz)
FoMs	**154.7dB**	153.7dB	152.2dB	132.1dB	148.6dB	108.6dB	116.6dB
FoMw	**1.16 pJ**	147 pJ	11.6 pJ	10.3 pJ	4.27 pJ	37.3 nJ	135 pJ
Area(mm^2)	**0.06**	6	6	0.025	0.135	0.36	0.015

*DC SNR, corrected by 2√2 when calculating FoM　**Estimated from noise floor

$$\text{FoMs} = \text{SNDR} + 10\log\left(\frac{\text{BW}}{\text{Power}}\right) \qquad \text{FoMw} = \frac{\text{Power}}{2^{\text{ENOB}} \times 2\text{BW}}$$

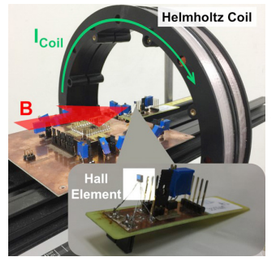


Fig 4. Application with magnetic field sensing

3
4

Fig 3. Comparison Table