Design Group
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適用於 LC 振盪器之長除數分數型倍數延遲鎖定迴路

A Fractional-N LC-VCO-based Multiplying Delay-Locked Loop with Large Multiplication Factors

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研究領域
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作品摘要

隨著技術的進步，高性能時脈系統的規格越來越嚴苛。一個運用震盪器之重整校正技術的鎖相迴路能簡單且有效地達成低雜訊之效能，其架構如：次諧波注入式鎖相迴路（SI-PLL）和倍數延遲鎖定迴路（MDLL）。

對於實際的高頻應用上，由於石英振盪器一般都操作於幾十兆赫（MHz），較大的除數是不可避免的。因此，此架構之頻率合成器將面臨一些問題如下：

1. 對於 SI-PLL，因本身的注入強度較弱，而造成不明顯地注入重整效果，或受太窄的鎖定範圍影響，導致失鎖狀態。
2. 對於 MDLL，雖然能打斷內部之震盪器，而有較強的重整校正效果。但此架構在本質上只能使用環振盪器來實現，受限於較低參考頻率所導致的窄頻寬影響，即便用週期性取代第地方式仍無法有效地抑制此環振盪器所產生的累積性抖動。
3. 此震盪器之重整校正技術一般僅能實現於整數型的鎖相迴路。

此外，上述兩種架構基本上僅適用於整數型，無法直接應用於分數型頻率合成器。為了移除此問題，我們提出了一個適用於 LC 振盪器之長除數分數型倍數延遲鎖定迴路，同時實現低雜訊和低功率分數型頻率合成器。

在本作品中，我們起初嘗試直接加多工器（MUXs）於輸出端以打斷原先之震盪器，但實現上卻因為此 MUXs 的加入，導致訊號之傳輸路徑產生低通的效果，進而衰減輸出端的振幅使得原先 LC-VCO 之相位雜訊上升，因此即使此架構可達到較大的頻寬，也將會因輸出振幅下降而惡化相位雜訊，如此將使得此方法不可行。後來，我們嘗試將此 MUXs 外加於主動元件的汲極端，如此一來，此外加等效電阻將會使得原先主動元件在振盪過程中，有更多時間操作於三極管區而導致較少的閃爍雜訊。除了可從低頻中看到抑制的效果，更可看出在 1MHz 的偏移頻率上，不會被其外加等效電阻惡化，此一特性巧妙地解決前段所提出的問題。簡言之，此全新之 LC 振盪器其特色除了對本身閃爍雜訊之抑制，還能巧妙地打斷原先的振盪狀態並適用於 MDLL 架構中以增加迴路頻寬，進而實現低雜訊低功耗之頻率合成器。

此外，加入一數位時間轉換器以調變參考時脈的延遲時間的概念來實現分數型操作。此處更結合再量化的三角積分調變器，可將 DTC 的增益誤差所導致的雜訊作重整至高頻，以實現更好的分數型性能。

本設計之分數型 MDLL 使用 TSMC 40nm 製程，核心面積為 0.2mm^2。因為使用於 MDLL 架構，因此所提出的 LC 振盪器操作於 5.12GHz 可被優化至僅耗 0.83mW，在 0.9V 電源下。在除數為 128 下，所提出之 MDLL 架構可達到之頻寬約為 15MHz 左右，而輸出訊號從 10kHz 到 30MHz 積分的均方根抖動量分別為 177fs（整數型）和 326fs（分數型）。隨著除數降至 64，所提出的 MDLL 可以實現更好的質量因數為 -254.2dB，其差別主要是由於參考時脈在 40MHz 時性能相對較差。

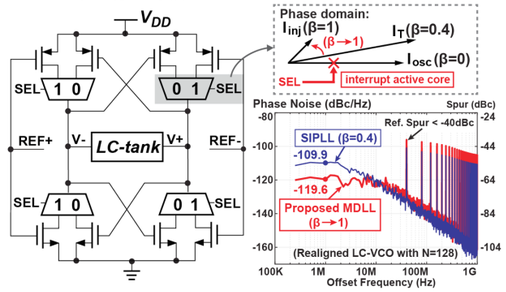

圖 1. 提出之 LC-VCO 適用於 MDLL 架構與模擬結果

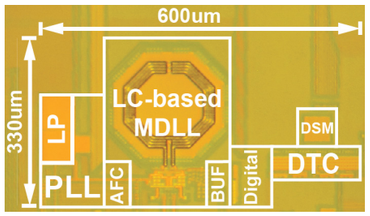

圖 2. 提出之分數型倍數延遲鎖定迴路晶片圖

Abstract

With the advancement in technology, the demand is increasing for high-performance frequency synthesizers with low power consumption. A phase-locked loop（PLL）with the VCO realignment technique is simple and effective to achieve superior phase noise, such as subharmonically injection-locked PLLs（SIPLL）and multiplying delay-locked loops（MDLL）.

For practical high-frequency applications, the larger frequency multiplication factor（N）is inevitable because the operation frequency of crystal oscillator is typically in the range of tens-of-MHz. Therefore, there are some challenges as follow:

1. For the SIPLL, it imposes a great challenge as we choose a high-Q LC oscillator with a larger frequency multiplication factor because the substantial narrow lock-in range causes unapparent realignment or even unlock state.
2. The strength of the realignment of the MDLL is stronger than the SIPLL by means of interrupting the VCO completely once every reference period. However, the MDLL can only be operated with the ring-based VCO inherently. Therefore, the narrow loop bandwidth（BW）which is accompanied by the low reference frequency is not effective to suppress the noisy VCO.
3. The PLL with the VCO realignment technique can only operate in an integer-N mode.

To mitigate this problem, the new structure of an LC-VCO-based MDLL is presented to enhance the jitter performance with a large frequency multiplication factor. In this work, the proposed LC-VCO is suitable in the MDLL. By employing the proposed MUXs in the LC-VCO, it increases the loop bandwidth（BW）from 3MHz to 15MHz（nearly 0.4fREF）as well as flicker noise suppression. Moreover, the re-quantized delta-sigma modulator（Re-Q DSM）is combined with the prototype in order to reduce spurious tones and in-band noise, which come from the gain error of the digital-to-time converter（DTC）.

In order to replace the VCO edge by the reference signal（REF）, we attempt adding a couple of symmetric inverters as the path from the reference to output. However, the finite on-resistance of the MUX is put in series to the gate of the transistors in the LC-VCO so that the input path forms a low-pass filter to attenuate the VCO output signal significantly. The attenuated signal leads to weaker the conduction of the cross-coupled inverter pair, thereby giving rise to phase noise in VCO.

The adoption of the MUXs in series to the drain of the transistors in the LC-VCO can suppress flicker noise up-conversion by operating the transistor in the triode region for more fraction of time. This approach is well suited for our application due to another characteristic that the phase noise is not degraded at 1MHz. In conclusion, the proposed approach not only disables the active core of the LC-VCO periodically but also suppresses flicker noise while the 1/f^2 phase noise is not detrimental.

The proposed MDLL has been further implemented in a fractional-N operation by modulating the input clock by a DTC. Within the proposed MDLL, the bigger the realignment factor is, the more sensitive to be affected by the reference clock. Thanks to the Re-Q DSM technique, the spurious tones and the in-band noise, which come from the gain error of the DTC can also be shaped to the high frequency.

This work has been fabricated in a 40nm CMOS technology and occupies an area of 0.2mm^2. The proposed LC-VCO is optimized to minimize power consumption, as the in-band phase noise is relaxed by the MDLL architecture. The VCO consumes only 0.86 mW for a supply of 0.9V at 5.12GHz. The proposed MDLL with a large frequency multiplication factor of 128 exhibits an integrated jitter of 177fs（integer-N）and 320fs（fractional-N）with respective power consumption of 1.96mW and 2.61mW from a 0.9V supply at 5.12GHz. With the frequency multiplication factor of 64, it achieves the excellent FoMJ of -254.2dB.

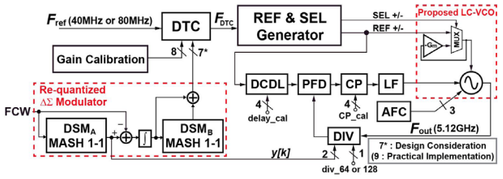

Fig 3. Block diagram of the proposed fractional-N MDLL