設計組
Design Group

D18-044

應用於第五代行動通訊系統之低損耗焊墊搭配靜電放電防護元件

Low-Loss I/O Pad with ESD Protection for 5th Generation Wireless Systems

隊伍名稱　春日部靜電防衛隊 Spring ESD Protection
隊　　長　彭柏維 / 臺灣師範大學電機工程研究所
隊　　員　賴玉瑄 / 臺灣師範大學電機工程研究所
　　林信希 / 臺灣師範大學電機工程研究所

指導教授

林群祐
臺灣師範大學電機工程學系

交通大學電子博士，現為臺灣師範大學電機工程學系副教授、臺灣靜電放電防護工程學會秘書長。曾任交通大學生醫電子轉譯研究中心助理研究員。

研究領域

射頻電路與其元件層級之靜電放電防護設計、高速數位電路與其元件層級之靜電放電防護設計、先進製程元件與其元件層級之靜電放電防護電路設計、生醫應用相關之積體電路設計、低電壓製程下可相容高工作電壓之積體電路設計。

作品摘要

隨著製程的演進，元件的尺寸大幅縮減，卻出現了嚴重的可靠度問題，電性過壓造成電晶體耐受能力大幅下降，其中靜電放電（Electrostatic discharge, ESD）是影響產品良率、製造成本、產品質量、產品可靠度和獲利率的最主要因素。奈米積體電路的製程技術不斷進步，電晶體的閘極氧化層厚度逐漸變薄、通道變短、接面變淺，但電路的崩潰電壓也隨之降低，只需幾伏特的靜電電壓便可打穿，遭受到靜電放電破壞的電路特性皆不可逆。靜電放電破壞造成積體電路或是電子產品全部約33%的損失，每年損失高達5億至50億美元。為了確保電子產品不被靜電放電所破壞，積體電路必須備有靜電放電防護電路，可靠度相關的國際標準也早被制定出來。台灣各大積體電路代工廠也為此設立可靠度部門以解決電性過壓與靜電放電破壞的問題，由此可見，半導體製程的良率與可靠度在近年來越來越受到關注與重視。雖然加入ESD防護元件能夠提供電路更佳的可靠度，但防護元件所產生寄生效應會影響內部電路。特別是防護元件的寄生電容嚴重地影響高頻電路的操作特性，如高頻信號的損失、輸入信號的延遲等，皆為必須克服的問題。隨著行動裝置、物聯網、4K影片、智慧家庭、AR/VR等新技術不斷發展，傳輸量每年不斷成長，必須滿足更高傳輸速率的需求。但現有的頻譜資源已飽和，需往更高頻的毫米波探測。目前通訊技術發展的主力－第5代行動通訊系統（5th generation wireless systems），有比4G快100倍的傳輸速度，更大的容量、低功率消耗、低延遲等優勢。K-band（18-27GHz）與Ka-band（27-40GHz）為第5代行動通訊系統應用的頻帶之一，然而ESD防護設計在極高頻的應用變得更加嚴苛，如果防護元件本身的寄生電容無法被消除，將使高頻響應被大幅地影響。因此本研究提出了新型的低損耗焊墊搭配靜電放電防護元件，具有高的ESD耐受度同時能將防護元件所造成的衰減移至低頻，使其適用於K/Ka-bands。傳統/新型設計皆被實踐在180奈米CMOS製程中，從量測結果與文獻比較可證實新型設計比傳統架構更適合應用在K/Ka-bands，此外，透過靜電放電耐受度測試，展現出新型設計的高ESD耐受度（HBM>8kV），遠超過現今業界的標準2kV，具有實用價值。

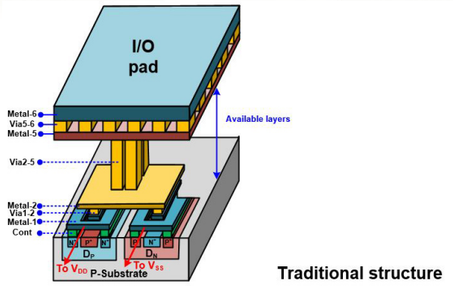

圖1. 傳統焊墊搭配靜電放電防護二極體之結構圖

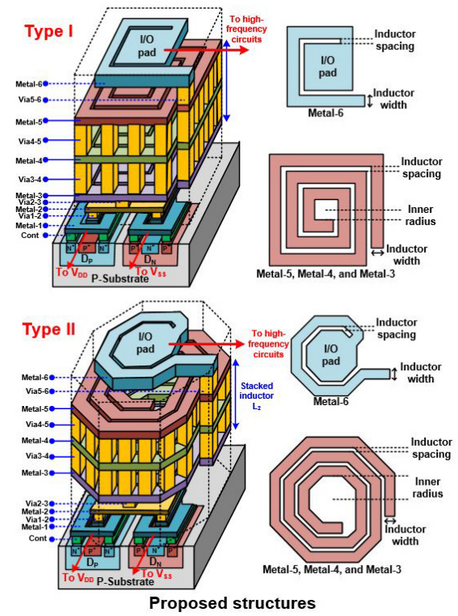

圖2. 新型焊墊搭配靜電放電防護二極體之結構圖

Abstract

Electrostatic discharge (ESD) is the most important consideration for the reliability of integrated circuits (ICs). The ultra-short channel length, ultra-thin gate oxide, and ultra-shallow junction seriously degraded the ESD robustness of ICs in nanoscale CMOS processes. The characteristics of circuits after ESD damage are irreversible. In order to increase the product yield and reduce the ESD damage, the ESD protection devices must be added in the ICs. Adding the ESD protection devices at input/output (I/O) pad can increase the circuit reliability. However, the parasitic effects of ESD protection devices will affect the circuit characteristics. In particular, the parasitic capacitance of ESD protection devices will seriously impact the high-frequency response of circuits, such as the signal loss from the I/O pad to ground. In order to effectively protect the circuits from ESD damage without losing the original characteristics, the parasitic capacitance of ESD protection devices must be minimized. The K-band (18-27GHz) and Ka-band (27-40GHz) are used in radar, broadband satellite, and 5G mobile communication systems. However, designing ESD protection devices is quite difficult in gigahertz bands. The parasitic capacitance of the ESD protection devices is one of the most important considerations for high-frequency applications. In addition, the parasitic effects of the I/O pad should also be taken into account. If these undesirable effects cannot be eliminated, the circuit characteristics will be distorted. The diode is often used as an ESD protection device because of the high current-discharging capability and the low turn-on voltage. In previous studies, in order to reduce the parasitic capacitance of ESD protection diodes, several special layout styles of diodes were proposed. However, the parasitic capacitance is limitedly reduced by adjusting the layout patterns of diodes. Therefore, this study presents two novel I/O pads with ESD protection dual-diodes to effectively reduce the signal loss and provide high ability of ESD protection.

The traditional I/O pad and proposed low-loss I/O pads have been compared in a 0.18 μm CMOS process for K/Ka-bands applications. The ESD protection design in I/O pad is an important consideration to have sufficient ESD robustness without losing the original characteristics of high-frequency. The measurement results confirm that the proposed structures have high ESD protection capability and lower signal loss than the traditional structure. Besides, the stacked inductor and dual-diodes are designed under the top metal plate to save chip area. The proposed low-loss I/O pads with ESD protection can achieve better performance for K/Ka-bands applications.

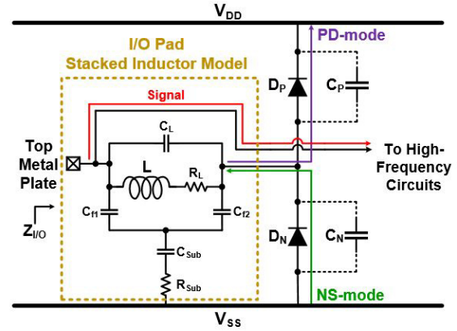

Fig.3 Proposed ESD protection scheme with stacked inductor and dual-diodes at I/O pad for high-frequency circuits

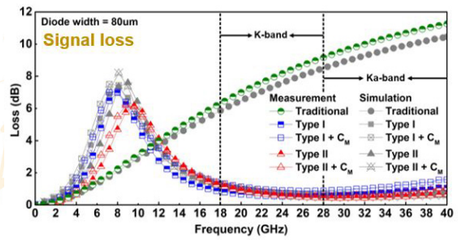

Fig.4 Measured signal losses of traditional and proposed structure with ESD protection diodes (Width=80um)