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採用不需時序錯誤偵測及修正之電壓調控技術的低功耗即時影像處理系統

A Low-Power Real-Time Video Processing System with a Detection-and-Correct-Free Voltage Scaling Technique

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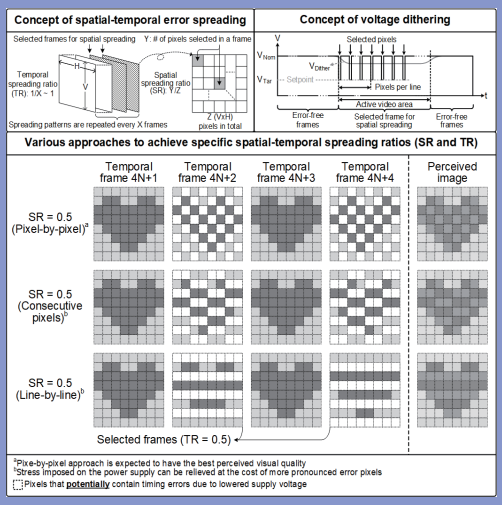
作品摘要

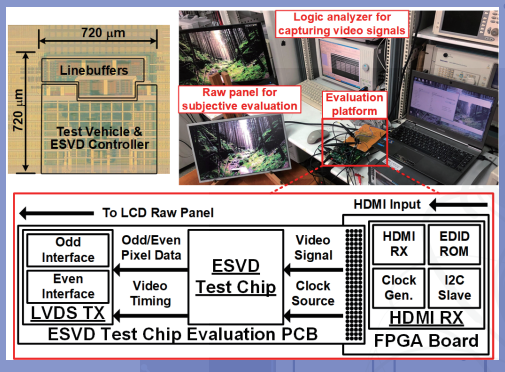
隨物聯網及穿戴式設備之興起，低功耗且高性能之影像硬體加速器漸受重視；然而，對影像品質需求的提升也使功耗更加惡化。近來雖有高能效影像硬體架構被提出，但基於電壓調控的低功耗技術於即時影像系統的應用仍很大程度受限於傳統的動態電壓調控技術（DVS）。由於在顯示器應用場景中，一旦開始輸出視訊後便無法隨意停止，此特性使常見於處理器系統之基於時序錯誤偵測及修正（TED與TEC）的自適性電壓調控（AVS）架構如Razor難以應用於即時影像系統中。少數現有技術雖有潛力突破此瓶頸，但相關技術皆因TED及TEC帶來額外的硬體及功耗開銷，且皆涉及具侵入性的演算法、架構及電路層面的修改而複雜化設計流程並增加時序收斂的難度。

本作品利用人眼視覺特性實現不需TED及TEC的電壓調控技術以回收設計餘裕，並以此技術實現一低功耗影像處理系統。所提之技術不需任何TED、TEC及其帶來的開銷，且不需要對影像處理資料路徑進行修改。圖一描述了所提之基於電壓抖動之空間/時域錯誤分散技術（ESVD），其概念是在選定的影格及其中的畫素降低操作電壓以減少動態功率消耗。不同於傳統AVS降低操作電壓後被動等待時序錯誤發生，所提之ESVD技術透過巧妙安排時序錯誤發生的影格及位置，並在運算至該位置時降低操作電壓，即可增進能效並透過視覺的低通特性來降低帶有時序錯誤的畫面對於主觀感受的影響。

本作品之測試晶片以聯華電子40奈米製程實現，其包含一即時視訊縮放引擎作為ESVD技術之載體。圖二是以測試晶片所建立之即時顯示系統，其可作為驗證平台並於LCD裸板上展示ESVD技術。如圖三所示，在不同操作條件下應用了ESVD技術後節能效益最高可達35%。主觀感受方面採用了ITU-T P.910標準中的失真等級評分，並以平均主觀意見分數（MOS）呈現。如圖四所示，應用了ESVD技術之後MOS皆高於4分。



▲ 圖一 本作品所提出之ESVD技術概念圖



▲ 圖二 基於ESVD測試晶片之即時視訊顯示系統

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研究領域

高效能數位積體電路設計、節能及容錯數位電路與系統設計、深度學習網路硬體與電路設計、電源管理積體電路、顯示器控制器積體電路

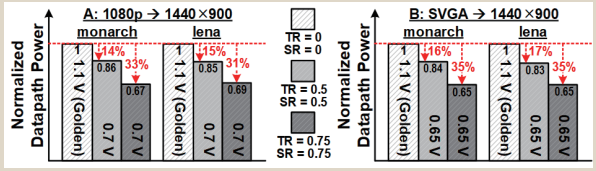
Abstract

Energy-efficient hardware accelerators for video processing are becoming favorable due to the increasing popularity of Internet of Things applications and wearable multimedia devices (e.g., wireless video sensor nodes and head-mounted displays). However, the demands of higher video quality adversely increase power and energy consumption. Recently, content-aware video systems with energy-quality scalability have been proposed to address these challenges. However, low-power techniques for video systems are still primarily confined to conventional dynamic voltage scaling techniques known to exhibit excessive design margins to account for the worst-case operating conditions. As video stream to the display can't be arbitrarily abrupted in a real-time display system, adaptive voltage scaling (AVS) based on timing error detections (TED) and corrections (TEC) (e.g., Razor) for processor systems are challenging to be applied to the real-time video systems. Although few known techniques could overcome these obstacles, they all require substantial algorithmic, architectural, and circuit-level modifications; these modifications are costly, invasive, incur timing closure difficulties, and complicate the design flow.

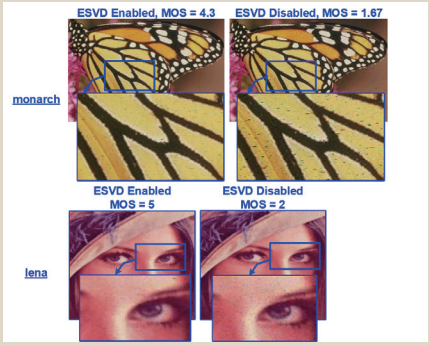
This project investigates the possibility that the design margin of a video processing datapath can be reclaimed without any overhead of the TED and TEC by exploiting the characteristics of human vision. The concept of the proposed spatial-temporal error spreading and voltage dithering (ESVD) technique for video processing datapaths are depicted in Fig. 3 The core concept of ESVD is to control how often a frame allows possible timing errors (i.e., temporal error spreading) and how many pixels in a selected frame can contain possible timing errors (i.e., spatial error spreading). These concepts are implemented by lowering the supply voltage to a setpoint when the datapath is processing these pixels, thus improving the energy efficiency.

Unlike conventional AVS that reduces the supply voltage and passively waits for timing error to happen (and then correct it), the ESVD actively allocates the locations allowed for the timing errors to occur. These cleverly distributed timing errors can then be automatically resolved by leveraging the persistence of vision and the human eye's tendency to mix pixels nearby.

The test chip of this project, which includes a real-time video scaling engine as a test vehicle for ESVD, is implemented using UMC 40nm CMOS process. Fig. 2 shows the real-time display system based on the test chip, which serves as a verification platform and can be used to demonstrate the ESVD technique on a raw LCD panel. As shown in Fig. 3, the datapath power is maximally reduced by 35% under different operating conditions. The mean opinion score (MOS), according to the degradation category rating (DCR) method in ITU-T P.910, is used for subjective quality assessments. MOS is higher than four after enabling the ESVD, as shown in Fig. 4.



▲ Fig. 3 Power consumption reduction in the video datapath



▲ Fig. 4 Zoomed images reconstructed from the raw video signal and their MOS