D23-006

112Gb/s極短通道之四階脈衝振幅調變電壓模態收發器於二十八奈米CMOS製程

A 112Gb/s XSR PAM-4 Transceiver in 28nm CMOS

隊伍名稱｜快樂串行解串組
Happy SerDes

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研究領域

超高速有線通訊傳收機、光纖通訊介面、鎖相迴路及其應用、毫米波無線通訊傳收機

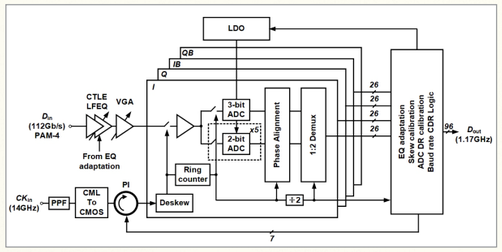
作品摘要

近幾年來，由於晶片的系統愈做愈大，在一個系統之中，存在許多裝有不同晶片功能的封裝，這些封裝中的計算引擎彼此需要頻繁地做資料交換，因此extra-short reach (XSR) 的SerDes應用逐漸成為主流的趨勢，其它像是AI/ML，HPC或是optical的應用也需要用到XSR SerDes的技術；相比於LR的應用，XSR的應用由於通道損耗較小，在Nyquist rate頻率下通道損耗大約不超過6dB，因此在晶片端不需要使用過多的功耗去做訊號能量復原的動作，因此XSR的SerDes講求在低功耗運作。

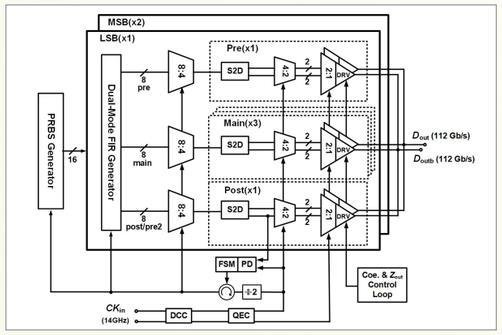
以2021年發布的兩篇ISSCC做為參考，其TRX在7奈米的製程下分別達到的power efficiency為1.7pJ/bit及1.55pJ/bit，因此本計畫旨在開發出一個相同傳輸速率 (112Gbps) 及相同應用場景 (XSR) 的SerDes晶片，並且其創新的架構預計可以在28奈米的製程下，TRX所消耗的power efficiency小於2.52pJ/bit。

圖一為112Gbps接收端架構圖，使用4個3-bit加上20個2-bit的sub ADC，以達到更多的error資訊量，進一步提升CDR的表現，並且其相比於傳統架構需解碼3 bit的溫度計碼，此架構可以直接解出二進位碼，並且放寬類比前端電路的負載，因此可以有效地降低功耗，其餘的直流偏移、等化器自適應、時脈偏移校正皆包含在降速後的數位電路中，以抵抗晶片的溫度、電壓及通道長度變異。

圖二為112Gbps發射端架構圖，採用了四分之一速率的時脈，將4:1多工器分解為4:2多工器和2:1多工器，分別採用同相和正交相位時脈以減少輸出負載。2:1多工器與驅動器合併，以減少最高速網路的數量。3-tap有限脈衝濾波器位於8:4多工器之前，並可根據不同通道配置 (α-2, α-1, α0) 和 (α-1, α0, α1) 等不同tap係數。透過感測由不同時脈相位編碼4:2多工器之平均輸出電壓，加入占比校正 (DCC) 和相位誤差校正電路 (QEC)，並進行自動校準。



圖一 112Gbps RX 架構圖。



圖二 112Gbps TX架構圖。

Abstract

In recent years, as chip systems have been growing larger, there are die-to-die communication in a large system. The computational engines in these packages need to exchange data frequently. As the result, the application of ultra-short reach (XSR) SerDes has gradually become a mainstream trend. Other applications such as AI/ML, HPC, and optical also require the use of XSR SerDes technology. Compared to long reach (LR) applications, XSR one has lower channel loss typically not exceeding 6dB at the Nyquist rate frequency. Therefore, there is no need for excessive power consumption at the chip end to do the equalization to recover the channel loss. Therefore, XSR SerDes emphasizes the low-power operation.

In the prior art of two ISSCC papers published in 2021, the power efficiency achieved by TRX in a 7-nm process was 1.7pJ/bit and 1.55pJ/bit, respectively. Therefore, the goal of this project is to develop a SerDes chip with the same data rate (112Gbps) and the same application scenario (XSR) while consuming less power. The innovative architecture of the chip is expected to achieve a power efficiency of less than 2.52pJ/bit in a 28-nm CMOS process.

Figure 1 shows the architecture of 112Gbps receiver. It utilizes four 3-bit sub ADCs and twenty 2-bit sub ADCs to capture more error information, thereby further enhancing the performance of the clock and data recovery (CDR). Compared to traditional architectures that require decoding of 3-bit thermometer codes, this architecture directly decodes the binary code and relaxes the load on the analog front-end circuitry, effectively reducing power consumption. Other calibration function such as DC offset calibration, equalizer adaptation, and clock skew calibration are included in the low-speed digital circuit to tolerate temperature, voltage, and channel loss variations in the chip.

Figure 2 shows the architecture of 112Gbps transmitter. It adopts a quarter-rate clocking scheme while disassembling the 4:1 MUX into 4:2 MUX and 2:1 MUX stages with in-phase and quadrature-phase clocks, respectively, to reduce the output loading. The 2:1 MUX is merged in the driver unit to reduce the number of full-rate nets. The 3-tap FIR is put in front of the 8:4 MUX and can be configured between (α-2, α-1, α0) and (α-1, α0, α1) modes for different channels. The duty-cycle correction (DCC) and quadrature-phase error correction (QEC) units are included with automatic calibration by sensing the average output voltage of a replica 4:2 MUX cell which is sequentially encoded as different clock patterns.

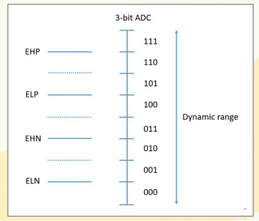


Fig.3 Concept of 3bit ADC decoder.

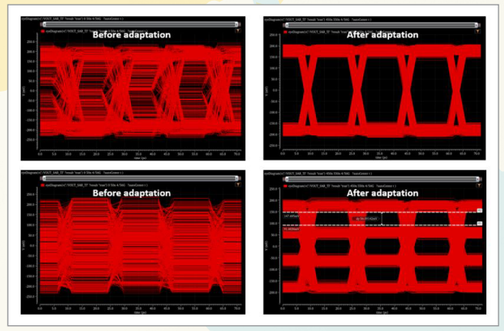


Fig.4 RX adaptation result.