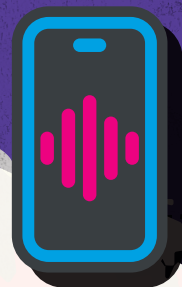D23-017

支援進階影像模式之整合式超音波數位訊號處理器

A Fully-Integrated Ultrasound Imaging Processor Supporting Advanced Modes for Hand-Held Devices

隊伍名稱｜超音特波隊2
The Ultrasoundibles 2

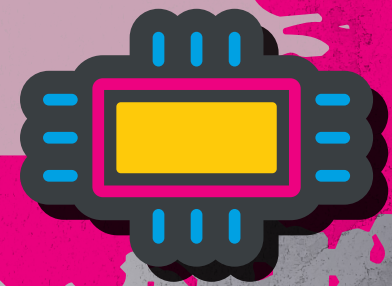隊　　長｜駱奕霖 / 臺灣大學電子工程學研究所
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研究領域
AI晶片設計、基頻通訊積體電路、生醫訊號處理晶片設計

作品摘要

超音波成像技術相較於其他醫學成像技術，具有低成本和非侵性的優點。近年來手持式裝置的發展改變了人類診斷的方式，其可攜性使醫生可以實現快速遠程的臨床決策，並使家用超音波成像裝置普及。超音波成像包含的內容可分為兩種模式：標準模式和進階模式。標準模式 (包括灰階模式、彩色都卜勒和功率都卜勒) 用於顯示組織的橫向截面和血流的特徵。相比之下，進階模式 (包括向量流和彈性成像) 可以提供更準確的流速和額外的組織硬度。組織硬度通常與病變緊密相連，例如乳癌與肝硬化的嚴重程度正比於組織的硬度。由此可見進階模式的重要性，然而目前文獻上還未有支援進階模式的超音波處理器架構。

此作品提出了世界第一顆支援進階影像模式之整合式超音波數位訊號處理器。此處理器支援所有模式的即時成像，通過演算法架構的最佳化，此作品提供比目前最先進的設計更低的複雜度和功率。所提出的演算法流程主要由五個模組組成，如圖一所示，包含平面波束成型、都卜勒訊號處理、參數估計、速率估計與影像後處理。演算法優化包含：(1) 利用發射延遲分解和不同發射角度發射延遲的公差，多角度平面波束成型的延遲儲存數量相較於總延遲儲存數量降低了99.8%。(2) 通過調轉傳統彈性演算法的處理順序，並加入所提出的粗略延遲查找法和低複雜度插值法，所需存儲量減少了78.1%。硬體優化包含：(1) 採用層的波束成型技巧，丟棄不需要的回波訊號以容納後面獲取的回波訊號來最小化儲存量，儲存量減少了93.8%。(2) 彩色、向量流、功率都卜勒和彈性模式共用自相關器，速度估計器面積下降25%。(3) 支援交錯發射技巧，通過交錯方式重新排列兩種模式的發射序列，使進階模式達到即時影像每秒30張影像的幀率。

本設計使用40-nm製程，晶片面積為5.5mm^2，供電範圍為0.63-0.91伏特，操作頻率範圍為100-200MHz，消耗功率範圍為30.7-169毫瓦。目前文獻上最佳的設計，在只有支援標準模式的情況下，在操作頻率為40MHz下消耗超過1瓦。相較於過去最佳設計，本設計在波束成型速率提高了20.3倍，消耗功率降低了6.7-36.6倍，面積也只有60%的大小。
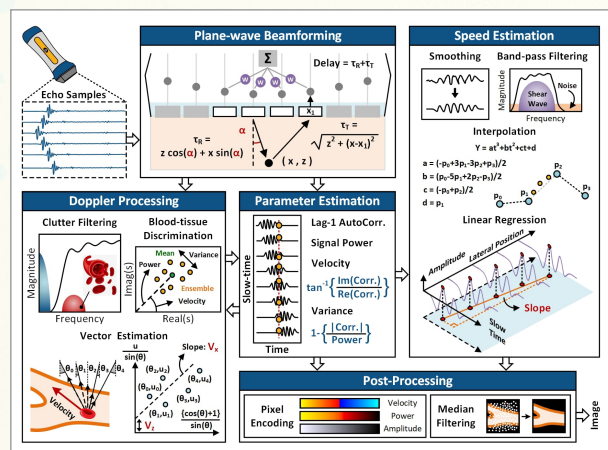
圖一 超音波成像流程圖。

Abstract

Hand-held ultrasound has changed the way for human diagnosis. Its portability enables remote and fast clinical decision-making. Ultrasound imaging can be categorized into two types of modes: standard and advanced. The standard modes (including B-mode, color Doppler, and power Doppler) are used to show the cross-sectional view of the tissues and the characteristics (velocity and reflection intensity) of the blood flow. In contrast, the advanced modes (including vector flow and elastography) display more accurate flow velocity and tissue stiffness, at a cost of higher computational complexity with a higher beamforming rate. Dedicated VLSI solutions for hand-held ultrasound have been developed for the standard modes, but processors supporting the advanced modes have not been demonstrated.

This work demonstrates the first fully-integrated ultrasound imaging processor supporting advanced modes. Fig. 2 shows the system architecture for the proposed ultrasound imaging processor. The processor consists of a planewave beamformer, a Doppler engine, a speed estimator, a parameter estimator, a memory bank, an encoder, and a median filter. Algorithm-architecture co-design is applied to optimize the design. Implementation complexity for beamforming is significantly reduced with the reduced stored delay size. The proposed elastography flow also largely reduces the storage size of shear wave data. Interleaved firing enables real-time imaging for advanced modes. For hardware optimization, low-complexity Catmull-Rom interpolation is applied, saving 79% area of the interpolator. The autocorrelator can be shared by color Doppler, vector flow and elastography imaging, reducing the speed estimator area by 25%.

Fabricated in 40-nm CMOS, the chip integrates 4.7M logic gates in core area of 3.24mm^2. The power consumption is 30.7-169mW at 100-200MHz from a 0.63-0.91V supply. The state-of-art ultrasound imaging processor only supports the standard modes, consuming 1124.4mW at a clock frequency of 40MHz. This work achieves a 20.3x higher beamforming rate with 6.7-to-36.6x lower power consumption. It also has 60% lower hardware complexity (in terms of gate count), in addition to the capability for supporting advanced modes.
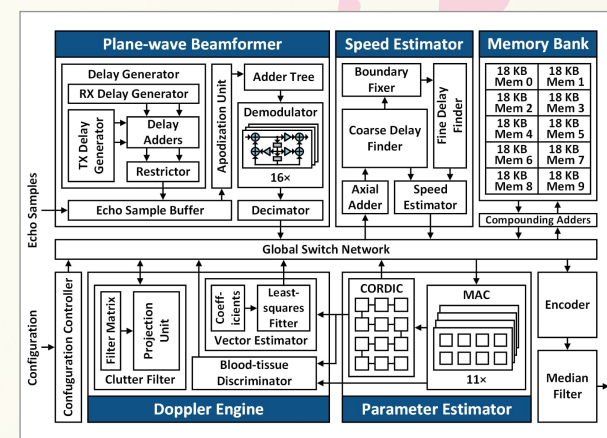
Fig.2 System architecture for the proposed ultrasound imaging processor.