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使用隔離式氮化鎵閘級驅動器解決碳化矽應用於高溫、高功率和高切換頻率之驅動問題

Using GaN-based Isolated Gate Drivers to Solve SiC Driving Problems for High Temperature, High Power and High Switching Frequency Applications

隊伍名稱｜閘級驅動器
GATE DRIVER

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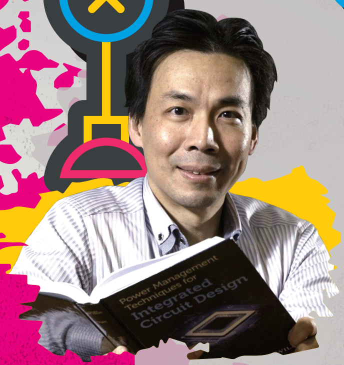

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研究領域

VLSI、低功率電路設計、混合訊號電路設計、電源管理IC設計

作品摘要

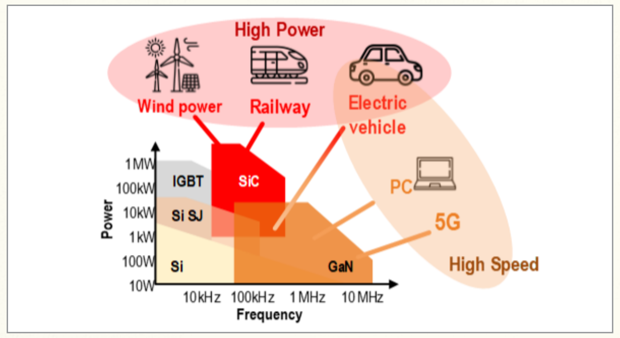
在環保議題及國際對碳排放限制的推動下，電動車的發展正在快速邁向成熟，因此應用於車電系統的元件是否可以耐高溫高壓變得十分重要。而SiC功率元件具有低阻抗和良好的耐溫性，另外還有高阻斷電壓和低損耗的優點，因此在電動車、鐵路和風力發電等高功率系統應用中有更好的性能。

然而，SiC功率元件大多使用在高溫高壓或是高功率的環境，因此其閘極驅動器必須能夠耐高溫，另外快速切換會對系統產生共模瞬態(Common-Mode Transient，CMT)的影響，進而導致訊號傳輸錯誤。最後還需要使用負壓關斷才能關閉完全，因此提出使用隔離式閘極驅動器來克服上述問題。

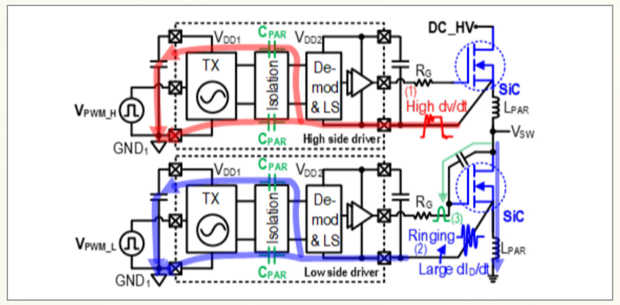
本作品選擇電容式的架構，其隔離層的材料由二氧化矽組成，特點是介電強度高，因此有良好的隔離強度。但是對於電容式來說，由於雜訊和訊號使用相同的傳輸路徑，所以對訊號的傳輸阻抗應較低，而對雜訊的傳輸阻抗較高。然而，有一些雜訊會被傳輸到RX電路，導致訊號傳輸錯誤。因此提高CMTI對於電容式隔離閘極驅動器非常重要。

1. 提升抗共模干擾度的包絡檢測技術：此提升抗共模干擾度的包絡檢測技術由轉阻放大器、高速比較器和解調變以及保護邏輯的電路所組成。其中，轉阻放大器具共模電流消除技術，以避免輸出訊號超出高速比較器的輸入共模範圍，之後再經由的包絡檢測技術解調變。
2. 低靜態電流電平轉換器：此架構可以產生負壓來關斷SiC MOSFET，所以不須外接一個電壓源，並且不會一直有靜態電流流向地，因此可以降低功耗和提升效率。
3. 四段電流驅動技術：藉由偵測SiC MOSFET的臨界電壓，分段供給SiC不同的驅動電流，可以減少振鈴效應同時縮短SiC MOSFET的開關時間，降低開關損耗。

本團隊所提出的基於GaN的隔離式SiC MOSFET閘極驅動器具有高達1600Mbps的高資料傳輸率和低傳播延遲(7ns)，並可以實現109kV/μs的壓擺率，同時有高達282kV/μs和211kV/μs的CMTI。在FSW=100kHz且VIN從800V變為1700V時，半橋隔離式DC-DC轉換器的效率可保持高於90%，當VIN=1700V、VIN=1200V和VIN=800V時，最高效率分別達到97.1%、98.1和98.6%。



圖一 不同類型半導體的應用範圍。



圖二 共模瞬態擾動的影響路徑。

Abstract

The development of electric vehicles is rapidly progressing due to environmental concerns and international regulations on carbon emissions. As a result, it is crucial for the components utilized in vehicle power systems to be capable of withstanding high temperatures and voltages. SiC MOSFETs offer low impedance, excellent temperature resistance, high blocking voltage, and low losses, making them ideal for high-power applications like electric vehicles, railways, and wind power generation.

However, SiC MOSFETs are predominantly employed in environments characterized by high temperatures, high voltages, and high power levels. Consequently, their gate drivers must be capable of enduring elevated temperatures. Furthermore, rapid switching can affect the Common-Mode Transient (CMT) response of the system, leading to signal transmission errors. To address these challenges, the utilization of isolated gate drivers with negative voltage shutdown capability is proposed.

In this study, a capacitive isolated gate driver is selected, with the isolation layer comprising silicon dioxide, known for its high dielectric strength and excellent isolation properties. In the case of the capacitive isolated gate driver, as the noise and signal share the same transmission path, it is necessary to have lower transmission impedance for the signal and higher transmission impedance for the noise. Nonetheless, some noise may still be transmitted to the RX circuit, resulting in signal transmission errors. Hence, enhancing the Common-Mode Transient Immunity (CMTI) of the capacitive isolated gate driver is crucial.

1. Improved CMTI Envelope Detection Technique
   This improved envelope detection technique consists of a transimpedance amplifier, a high-speed comparator, demodulation, and protection logic circuits. The transimpedance amplifier employs common-mode current elimination technology to prevent the output signal from exceeding the input common-mode range of the high-speed comparator. Subsequently, the signal is demodulated using the envelope detection technique.
2. GaN-Based Low IQ Level Shifter and Negative Voltage Generator
   This architecture generates a negative voltage to turn off the SiC MOSFET, eliminating the need for an external power supply. It also prevents a continuous static current flowing to the ground, thereby reducing power consumption and improving efficiency.
3. Quad Drive Control Technique
   By detecting the threshold voltage of the SiC MOSFET, different driving currents are supplied in segments, reducing the ringing effect and shortening the switching time of the SiC MOSFET, thereby reducing switching losses.

The proposed GaN-based isolated SiC MOSFET gate driver has high data rate which is up to 1600Mbps and low propagation delay (7ns). It achieves a slew rate of 109kV/μs and improve the positive and negative CMTI to 282kV/μs and 211kV/μs, respectively. At FSW = 100kHz, the efficiency of half-bridge isolated DC-DC converter can be kept higher than 90% when VIN changes from 800V to 1700V and the peak efficiency reaches 97.1%, 98.1 and 98.6% when VIN = 1700V, VIN = 1200V, and VIN = 800V, respectively.

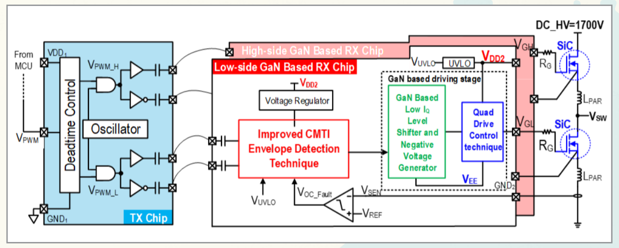


Fig.3 Architecture of proposed isolated SiC MOSFET gate driver.