## D24-033

# 具減少14.7倍拖尾電流消耗與減少37.0%反向傳導損耗之單晶片低漏電交叉耦合氮化鎵驅動器

**A Monolithic Low-ILEAK Cross-Coupled GaN Driver with 14.7X Reduction in Tailing Current Loss and 37.0% Reduction of Reverse Conduction Loss**


隊伍名稱｜GaN什麼東西 GaN What

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臺灣大學電機工程學士、碩士、博士，現為陽明交通大學電機工程學系講座教授以及IEEE Fellow。曾於1996至1998年任臺北飛利浦公司兼職IC設計人員，1998至2000年任Avanti擔任項目經理，從事電源管理IC的設計。成立陽明交通大學混合信號和電源管理IC實驗室，在IEEE頂尖期刊 ( JSSC及TPE ) 和會議 ( ISSCC及VLSI symposium ) 上有卓越的貢獻，並擁有多項專利。


**研究領域**

電源管理積體電路設計、混合訊號電路設計、液晶顯示器 ( LCD ) 驅動器設計、氮化鎵驅動器設計

## 作品摘要


人工智慧、串流媒體與自駕車等技術，都仰賴數據中心提供強大的算力支持與資料存儲空間。然而目前數據中心建置商面臨電力供應不足的重大挑戰，因此提高數據中心的能源使用效率成為各廠商著眼點，其中第三代半導體氮化鎵 ( GaN ) 廣受關注，使用GaN為基底的高功率密度功率轉換器建置數據中心，可以達到小體積與高功率效率，為當前挑戰帶來曙光。

針對高頻率、高功率密度功率轉換器，過往研究多著墨於GaN和矽相比的三大優勢：較小的接面電容、導通電阻和無反向恢復損耗。然而我們發現GaN要達到高功率效率，還有兩大待解問題:元件本身的漏電問題、板上實現產生的大量寄生元件導致效率與可靠度下降，其效應在高頻運作下尤為顯著。

為解決兩大問題，本作品提出單晶片GaN驅動器的解決方案，針對提高效率我們做了三點改善:透過單晶片設計顯著減少寄生元件、雙模式電壓穩壓器與自供電驅動增強技術 ( SPDE ) ；而針對漏電問題我們提出兩點設計：交叉耦合架構、短週期負電壓技術 ( SPNV ) 。

整體架構如圖一所示，圖中標明了四個特點：

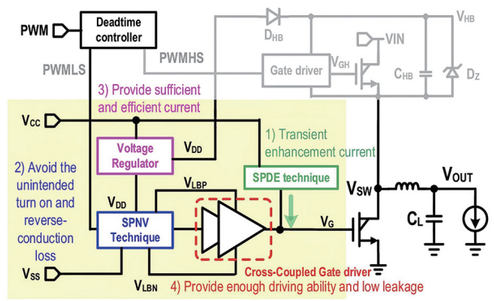
1.利用SPDE提供兩路不同電流，以增強VG的瞬態響應，並且在穩態時自動進入睡眠模式，以提升整體電路的效率。

2.利用SPNV提供短時間的負電壓，以避免米勒耦合效應導致功率元件切換時，下橋功率元件意外開啟，並減少死區期間內的反向導通損耗。

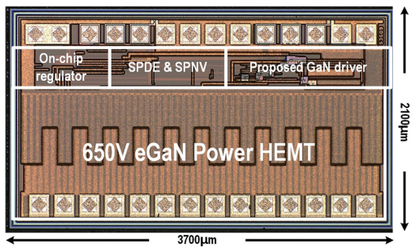
3.雙模式電壓穩壓器包含自動增加驅動電流以改善瞬態響應的強模式；以及在負載需求顯著下降的穩態啟動的高效率模式，提供所需的小電流負載以提高效率。

4.單晶片低漏電流交叉耦合氮化鎵驅動器運用VG=0V狀態下，E-GaN關閉與D-GaN開啟沒有漏電流的特性，加上交叉耦合自充電泵機制降低傳統多級幫浦架構複雜性，達到改善漏電流的目標。

本晶片使用GaN-on-Si製程製作，VD=100V、VCC=7V、VDD=6V、fsw=50MHz條件下的驅動器開啟測量波形顯示，SPDE減少14.7倍的尾電流效應功率損耗；和過往架構相比，提出的SPNV減少37.0%的反向導通損失。整體驅動器設計提供5A的驅動電流和240W的輸出功率，從負載與功率效率關係圖中 ( 如圖三所示 ) ，可見負載從1A到5A的狀況下，效率改善在10%以上，達成前述小體積與高功率效率的目標。


圖一 系統架構圖。




圖二 利用GaN-on-Si製程的晶片照片。

## Abstract


Artificial intelligence, streaming media, and autonomous vehicles rely on data centers to provide high computing power and data storage space. Recently, data center builders have faced significant challenges due to inadequate power supply. Therefore, improving power efficiency has become popular for data center operations. Due to the advantages of high power efficiency and compact size, third-generation semiconductor gallium nitride (GaN) can become a good candidate for high-power-density power converter design in the data center application.

Previous research has extensively explored GaN's three significant advantages compared to silicon in high switching frequency and high power density converter design: smaller junction capacitance, lower on-resistance, and absence of reverse recovery losses. However, we've found two severe issues for GaN to achieve high power efficiency: GaN device leakage and rising substantial inductive and resistive parasitic elements in board-level implementation. Those effects degrade GaN circuit efficiency and reliability, especially at high frequencies.

To address these challenges, we propose a monolithic GaN driver solution. There are three features for efficiency improvement: a monolithic design for reducing parasitic elements, a dual-mode voltage regulator, and self-powered driver enhancement (SPDE). As for the leakage improvement, a cross-coupled architecture and Short-Period Negative Voltage (SPNV) technology are proposed.

The whole proposed architecture is illustrated in Figure 1, which highlights four features:

1. SPDE provides two different paths of currents to enhance the transient response of VG. Specifically, the SPDE block will provide another diving path from a higher supply voltage VCC to avoid voltage degradation of VDD due to the coupling effect in the high switching operation. Moreover, it automatically enters sleep mode during the steady state to improve overall circuit efficiency.
2. Using SPNV to provide short periods of negative voltage prevents the Miller coupling effect from causing accidental activation of the low-side switch. It reduces reverse conduction losses during dead time and eliminates the shoot-through current.
3. A dual-mode voltage regulator includes strong and high-efficiency modes. The circuit automatically increases the drive current in the strong mode to improve transient response. Since the voltage regulator's load requirement drops significantly in the steady state, the high-efficiency mode provides a small current to maintain the load, reducing power consumption and improving efficiency.
4. A monolithic low-leakage current cross-coupled GaN driver that utilizes the zero-leakage characteristic of E-GaN off-state and D-GaN on-state under VG=0V, combined with a cross-coupled self-charge pump mechanism to reduce the complexity of traditional multi-level pumping structures, achieving the goal of reducing leakage current.

This chip is fabricated using GaN-on-Si technology, shown in Figure 2. Under VD=100V, VCC=7V, VDD=6V, and fsw=50MHz, the measured driver turn-on waveform shows that SPDE reduces the tail current effect power loss by 14.7 times. The proposed SPNV reduces reverse conduction loss by 37.0% compared to previous architectures. The overall driver design provides a driving current of 5A and an output power of 240W. With a load ranging from 1A to 5A, efficiency is improved by more than 10%, shown in Figure 3, achieving the goals of compact size and high power efficiency.

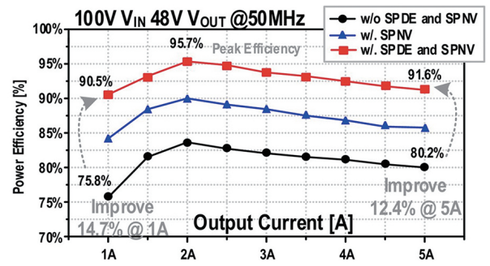




Fig. 3 The relationship between loading and power efficiency.