D24-038

一個只具有六個的比較器與PRTS檢查器之40-Gb/s的三階脈衝震幅調變接收機

A 98-fJ/b/dB 40-Gb/s PAM-3 Receiver with only Six Summer-merged Slicers and PRTS checker

隊伍名稱｜三階脈衝震幅調變接收機 PAM-3 Receiver
隊　　長｜林哲恩 / 臺灣大學電子工程學研究所

指導教授

劉深淵｜臺灣大學電機工程學系

臺灣大學電機博士，現為臺灣大學電機工程學系 / 電子工程學研究所特聘教授。曾任IEEE SSCS Taipei Chapter主席、IEEE Journal of Solid-State Circuits副主編、臺灣大學電子工程學研究所所長。

研究領域

混合式積體電路設計與應用、通訊積體電路設計與應用

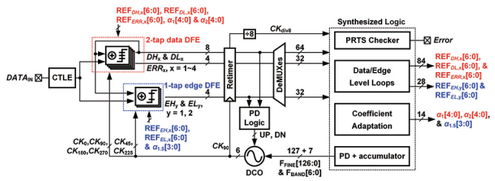
作品摘要

對於高損耗通道，多級脈衝振幅調變 (PAM) 信號被用於在各種有線通信系統中傳輸高速數據，例如四級PAM (PAM-4) 或三級PAM (PAM-3)。與非歸零 (NRZ) 信號相比，PAM-4信號可以實現較高的數據速率。然而，PAM-4信號具有較差的信噪比 (SNR) 並對信號的線性敏感。考慮到通道損耗、線性和信噪比，PAM-3信號被新一代的USB系統當作是一種替代方案。因此本篇希望以低功號的方式來實現USB4的資料速度要求。

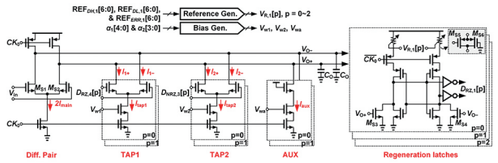
圖1展示了提出的PAM-3接收器。它包括CTLE、2-tap data DFE、1-tap edge DFE、再定時器 (Retimer)、PD邏輯、DCO、除以8的分頻器、解多路器 (DMUXes) 和一個合成電路。2-tap data DFE和1-tap edge DFE分別由時鐘CK_0 / CK_{90} / CK_{180} / CK_{270}和CK_{45} / CK_{225}驅動。對於2-tap data DFE，其輸出DH_x和DL_x分別表示取樣數據，ERR_x用於適應DFE的係數 (x=1~4)。1-tap edge DFE的輸出，EH_y和EL_y (y=1~2)，結合DH_x和DL_x用來實現PD邏輯。值得注意的是，PD邏輯直接控制DCO以減少迴路延遲。合成電路由提出的PRTS檢查器、位準校正迴路、係數適應電路、PD和一個20位累加器組成。PRTS檢查器的輸出信號Error用於計算比特錯誤率 (BER)。位準校正迴路生成二進制代碼$REF_{DH,x}$[6:0]、$REF_{DL,x}$[6:0]、$REF_{ERR,x}$[6:0]、$REF_{EH,y}$[6:0]和$REF_{EL,y}$[6:0]，用於生成dada和edge DFE的參考電壓。係數適應電路生成二進制代碼α_1[4:0]、α_2[4:0]和$\alpha_{1.5}$[3:0]，分別控制第一和第二data DFE的係數和edge DFE的係數。位準校正迴路和係數適應電路的邏輯實現使用SSLMS方法。PD和累加器生成溫度計代碼F_{FINE}[126:0]和F_{BAND}[6:0]，以控制DCO的頻率。

圖2展示了提出的比較器架構。它由一對差分對、六個電流源和三個regeneration latch組成。輸入的差動對M_{S1}和M_{S2}在此為DFE的加法器和三個regeneration latch的輸入級。由$M_{w1,p}$、$M_{w2,p}$和$M_{wa,p}$實現的六個電流源用來實現DFE回授的輸入，其中電流I_{1+}、I_{1-}、I_{2+}和I_{2-}由$D_{RZ,4}$[1:0]和$D_{NRZ,3}$[1:0]控制，分別用於抵消第一和第二後游標。最後為了保持I_{tap1}、I_{tap2}和I_{aux}的總和固定，增加了兩個輔助電流源I_{aux}。至於regeneration latch，其由兩個電壓-電流轉換器M_{S3}和M_{S4}、兩個交叉耦合反相器、兩個電壓控制可變電阻、兩個時鐘控制開關和兩個反相器組成。每個電壓控制可變電阻由M_{S5}和M_{S6}實現，並由差動電壓$V_{R,1}$[p]控制，其中p=0~2。與傳統電流積分的summer相比，我們提出的比較器沒不需要取樣保持電路。此外，更減少了DFE的回授路徑的時間。

最後這個PAM-3接收器採用TSMC 28奈米CMOS技術製造，具有0.12平方毫米的有效面積。供電電壓為0.9V和1V，分別用於合成邏輯電路和其他電路。這個PAM-3接收器在3^7-1的40Gb/s PRTS (偽隨機三元序列) 下的總功耗為90 mW。相較於最近的其他作品，我們的研究在類似或更大的通道損耗下實現了良好的FoM。此外，我們的作品中不需要TX FFE和被動電感器。因此，我們實現了更小的面積。



圖一 提出的PAM3接收機架構。



圖二 提出的比較器架構。

Abstract

For a high-loss channel, multi-level pulse amplitude modulation (PAM) signaling is used to transmit the high-speed data in various wireline communication systems; such as four-level PAM (PAM-4) or three-level PAM (PAM-3). Compared with the non-return-to-zero (NRZ) signaling, PAM-4 can achieve a higher data rate. However, PAM-4 signaling has a limited signal-to-noise ratio (SNR) and is also sensitive to signaling linearity. To trade off among the channel loss, linearity, and SNR, the specification of USB4 using PAM-3 signaling. Therefore, this work is aim to fulfill a low power PAM-3 receiver.

The proposed PAM-3 receiver consists of a two-stage CTLE, a two-tap data DFE, a one-tap edge DFE, a retimer, PD logic, a DCO, a divide-by-8 divider, demultiplexers (DeMUXes), and a synthesized circuit. The two-tap data DFE and the one-tap edge DFE are clocked by CK_0 / CK_{90} / CK_{180} / CK_{270} and CK_{45}/ CK_{255}, respectively. For the two-tap data DFE, its outputs, DH_x and DL_x, represent the sampled data and ERR_x is used to adapt the DFE's coefficients, where x=1~4. The outputs, EH_Y and EL_Y where y=1~2, of the edge DFE combine DH_x and DL_x to realize the PD logic. Note that the PD logic directly controls the DCO to reduce loop latency. The synthesized circuit is composed of a proposed PRTS checker, data/edge level loops, coefficient adaptation circuits, a PD, and a 20-bit accumulator. The output signal, *Error*, of the PRTS checker is used to calculate the bit error rate (BER). The data and edge level loops generate the binary codes, $REF_{DH,x}$[6:0], $REF_{DL,x}$[6:0], $REF_{ERR,x}$[6:0], $REF_{EH,y}$[6:0], and $REF_{EL,y}$ [6:0], to generate the reference voltages for the data and edge DFEs. The coefficient adaptation circuits generate the binary codes, α_1[4:0], α_2[4:0], and $\alpha_{1.5}$[3:0] to control the first and the second data DFE's coefficients and the edge DFE's coefficient, respectively. The logic implementations for the level loops and coefficient adaption circuits use the sign-sign least-mean-squares methods. The PD and the accumulator generate the thermometer codes F_{FINE}[126:0] and F_{BAND}[6:0] to control the DCO's frequency.

Fig. 3 shows the proposed PRTS-7 checker. It consists of three selectors, three decoders, a checker logic, and a toggle flip-flop. The DeMUXes will output 32 sets of the data, {DH'$_0$, DL'$_0$}~{DH'$_{31}$, DL'$_{31}$}, every clock cycle of CK_{div8}. The selectors will select 3 sets of the data, and the decoders will convert these data into the PAM-3 symbols denoted as S_n', S_{n-2}', and S_{n-7}'.

Then, the checker logic will check whether S_n' is equal to mod3(S_{n-2}'+2S_{n-7}'), and the toggle flip-flop will check CHKO. If CHKO is the logic high, which S_n' is not equal to mod$_3$(S_{n-2}'+2S_{n-7}'), the output signal, *Error*, will alter every clock cycle of CK_{div8}. If not, *Error* will be kept. Therefore, the BER of the receiver can be easily converted by measuring the time during *Error* is kept.

Fig. 4 shows the die photo of the proposed PAM-3 receiver. It is fabricated in TSMC 28-nm CMOS technology and has an active area of 0.12mm^2. The supply voltage of 0.9 and 1V are for the synthesized logic circuit and remaining ones, respectively. The total power dissipation of the PAM-3 receiver is 90-mW for the 40-Gb/s PRTS of 3^7-1 when the channel loss up to 23-dB at 12.8-GHz. Compared to recently work, our work achieves a good FoM with the similar or larger channel loss. In addition, the TX FFE and passive inductors are not required in our works. Therefore, the smaller area is achieved.

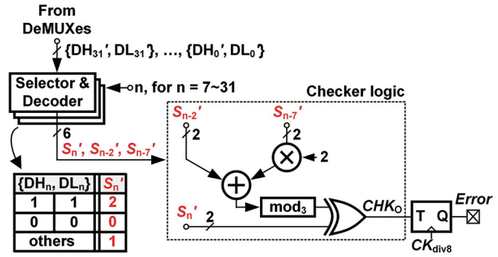


Fig. 3 PRTS7 checker.

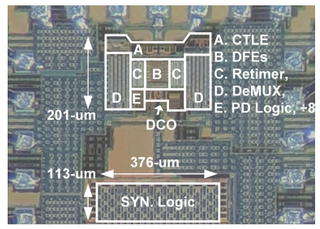


Fig. 4 Chip photo of the PAM3 receiver.