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應用於物聯網之超低功耗多通道多模式無線發射機

An Ultralow-Power Multi-Channel Multi-Mode Wireless Transmitter for IoT Applications

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研究領域

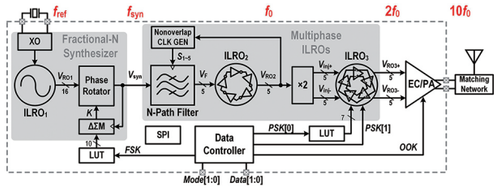
超低功耗射頻、類比與混合信號積體電路與系統設計，無線收發機、類比數位轉換器與鎖相迴路之低功耗技術，無線供電與獵能技術、生醫與感測器介面設計

作品摘要

物聯網系統應用在商業、醫療或工業的情況下，從健康監測傳感器、智能手機、以及到環境計算機的雲端運算等，這些物聯網設備僅具有十分有限的功耗預算，甚至必須使用無電池的能量收集方案。因此，物聯網的實現需要仰賴非常高效率的無線通訊技術，將需求一個無線收發機系統僅消耗極少能量、或甚至能夠從環境周遭中獲得補充，來增加物聯網裝置的使用時間，進而提供一個低成本、低維護人力的可靠解決方案。

因應物聯網概念的快速發展，無線感測節點必須具備低功耗、小體積之特性，本作品設計出一個超低功耗的無線電發射機，期望透過足夠的環境獵能技術供電，以顯著增加操作時間，實現自給自足的物聯網裝置。在所提出的無線發射機架構中，將專注於倍頻技術以及操作在低頻的頻率合成器和相位調製器的研發，避免再依賴傳統耗電的高頻鎖相迴路和本地振盪器的使用，進而突破現今技術之功耗瓶頸，以利達到大幅降低整體功耗的效果。此外，本作品亦具有多通道通訊能力以克服不同的路徑損耗和干擾，並且能夠支援多種主要廣泛應用在現代低功耗無線通訊和傳感器網路中的調變模式。

本團隊自行設計的晶片採用TSMC 90 nm CMOS製程，開發出雙級注入鎖定和倍頻技術的高效率與超低功耗433 MHz無線發射機。透過基於低頻相位旋轉的頻率合成器來支援多通道通訊和FSK調製，而由ΔΣ調製器產生的量化雜訊透過N路徑濾波器和兩個雙注入鎖定環形振盪器(ILRO)濾除。接著通過改變ILRO的自由運行頻率以產生相位差來實現相位調製。最後藉由高能效的電流模式D類邊緣組合功率放大器實現5倍頻放大進而產生所需的載波頻率。此發射機在0.75 V電源電壓下的功耗為870 μW並提供−7 dBm的輸出功率，在OOK/BFSK/QPSK調變可分別支援40/5/80 Mbps的數據傳輸速率。未來若能結合先進的環境獵能技術，這種節能高效的無線發射器可以顯著延長物聯網設備的電池壽命，實現一個能源自主物聯網系統。



圖一 超低功耗多模調變發射機系統架構圖。

Abstract

In applications of IoT systems in commercial, medical, or industrial contexts, from health monitoring sensors and smartphones to cloud computing for environmental computers, these IoT devices have extremely limited power budgets and may even need to use battery-free energy harvesting solutions. Therefore, the realization of IoT relies on highly efficient wireless communication technology, requiring a wireless transceiver system that consumes minimal energy or can even be supplemented by energy harvested from the environment to extend the usage time of IoT devices, thereby providing a reliable solution with low cost and low maintenance.

In response to the rapid development of the IoT concept, wireless sensor nodes must have low power consumption and small size. This work designs an ultra-low-power wireless transmitter with the goal of significantly increasing operating time through sufficient environmental energy harvesting techniques to achieve self-sustaining IoT devices. The proposed wireless transmitter architecture focuses on frequency multiplication technology and the development of low-frequency frequency synthesizers and phase modulators, avoiding the reliance on traditional power-hungry high-frequency phase-locked loops and local oscillators, thus breaking through the current power consumption bottleneck to greatly reduce overall power consumption. Additionally, this work features multi-channel communication capabilities to overcome different path losses and interference and can support various modulation schemes widely used in modern low-power wireless communication and sensor networks.

Our team designed the chip using TSMC 90 nm CMOS process, developing a highly efficient and ultra-low-power 433 MHz wireless transmitter with dual-stage injection locking and frequency multiplication technology. The multi-channel communication and FSK modulation are supported by a frequency synthesizer based on low-frequency phase rotation, while the quantization noise generated by the ΔΣ modulator is filtered out by N-path filters and two dual-injection locked ring oscillators (ILROs). Phase modulation is achieved by changing the free-running frequency of the ILRO to generate phase differences. Finally, a high-efficiency current-mode class-D edge-combined power amplifier achieves 5x frequency multiplication to generate the required carrier frequency. This transmitter consumes 870 μW at a 0.75 V power supply and provides an output power of −7 dBm, supporting data transmission rates of 40/5/80 Mbps for OOK/BFSK/QPSK modulation, respectively. In the future, if combined with advanced environmental energy harvesting technologies, this energy-efficient wireless transmitter can significantly extend the battery life of IoT devices, realizing an energy-autonomous IoT system.

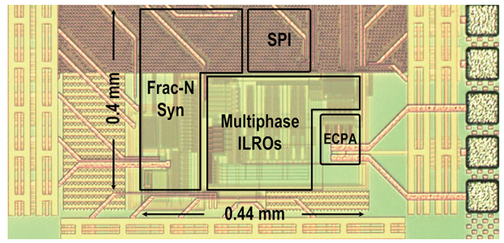


Fig. 2 Chip micrograph of the proposed transmitter.