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基於跨模態語意關聯之半導體精密檢測與分析技術

Cross-Modal Semantic Association-Based Semiconductor Precision Inspection and Analysis Technology



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研究領域

智慧物聯網、人工智慧、影像處理、深度學習。



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研究領域

涵蓋生醫工程、光聲成像、生物資訊、人工智慧、智慧感測裝置、仿生智能及 VR/AR/MR 技術整合。

作品摘要

隨著半導體製程持續微縮，晶圓廠在精密檢測上面臨日益嚴峻的挑戰。傳統人工顯微鏡檢測高度仰賴操作員的經驗與體力，效率有限且品質難以一致；現有AI方案雖能偵測缺陷位置，卻無法解釋成因，亦缺乏與機台硬體的整合。廠內各機台資料系統彼此孤立，工程師須耗費大量時間人工研判根因，製程回饋嚴重滯後。

有鑑於此，本作品提出 SemiScan——一套結合硬體改裝與邊緣端AI推理的智慧化晶圓閉迴路檢測系統，由三大創新構成。第一，非侵入式半自動顯微鏡改裝模組。以3D列印支架將步進馬達固定於現有手動顯微鏡的載台與焦距旋鈕，搭配自動對焦控制迴路，在不汰換既有設備的前提下升級為半自主檢測節點，大幅降低導入成本。

第二，多階段AI影像檢測與根因分析流程。系統在蝕刻後(AEI)對晶圓進行實體掃描，以物件偵測模型辨識電晶體幾何結構，透過視覺語言模型自動讀取晶粒座標，依量測結果逐一判定通過或失敗狀態。結果彙整後，由影像分類模型將缺陷分佈歸類為業界標準樣態，再透過檢索增強生成引擎結合製程標準作業程序與機台日誌推論根因，自動產出工程報告。全部推理均於本地邊緣伺服器執行，確保廠內資料安全。

第三，多智能體知識推理與製程回饋架構。系統以圖狀有限狀態機協調多個AI智能體，依據AEI檢測所得的缺陷樣態，回溯推理塗佈後(ACI)與顯影後(ADI)各製程節點的潛在根因，並在下一批次前提供前饋式製程補償建議，實現跨站主動控制。工程師可透過自然語言介面即時查詢缺陷歷程，系統亦於每批次後自動彙整完整報告，建立可追溯的製程知識資產。

SemiScan以低門檻的硬體改裝方案整合多模態AI推理與閉迴路製程回饋，縮短批次晶圓的人工檢測時間、提升線上缺陷攔截率，並將仰賴資深工程師的隱性知識數位化，使半導體製造從被動的事後品管邁向主動的即時補償，為中小型晶圓廠與研究單位提供可落地的智慧化升級路徑。



圖一 系統流程圖。

Abstract

As semiconductor fabrication advances toward smaller process nodes, wafer fabs face precision inspection demands that current workflows cannot meet. Manual microscope inspection depends on operator skill and endurance, yielding limited throughput and fatigue-induced variability across shifts. Existing software-only AI solutions can locate defects but cannot explain their physical mechanisms or interface with process equipment to trigger corrective action. Worse, process data remains siloed in incompatible formats, forcing engineers to manually correlate logs before hypothesizing a root cause—so feedback arrives too late to prevent yield loss within the same batch, reducing quality control to a reactive discipline.

This work presents SemiScan, an intelligent closed-loop wafer inspection system that unifies hardware retrofitting with edge-deployed multimodal AI, organized around three core innovations.

At the hardware layer, a non-invasive microscope retrofit module uses custom 3D-printed brackets to mount stepper motors onto a conventional microscope's stage and focus knobs, paired with image-contrast auto-focus. This converts legacy equipment into a semi-autonomous inspection node without permanent modification, targeting university labs, small-to-mid-sized fabs, and IC testing facilities that cannot justify purpose-built metrology systems.

For inspection and diagnosis, a multi-stage AI pipeline performs after-etch inspection (AEI): an object detection model identifies transistor structures while a vision-language model reads die identifiers and coordinates. Each transistor is evaluated against geometric criteria, and aggregated results are classified into standard defect patterns. A retrieval-augmented generation engine then cross-references SOPs and equipment logs to infer the responsible upstream step, producing a structured report with prioritized recommendations. All inference runs on a local edge server, ensuring fab data-security and air-gap compliance.

Closing the loop, a multi-agent reasoning architecture built on a graph-based finite state machine orchestrates agents that trace anomalies back to after-coat (ACI) and after-develop (ADI) inspection, issuing feed-forward compensation before the next lot enters production. Engineers query defect histories in natural language, and each cycle compiles a batch report, building a traceable institutional knowledge base.



Fig. 2 System structure.