D26-051

應用於112/224 Gb/s 超高速有線接收機之DSP架構設計

112/224 Gbps DSP for
Ultra-High Speed Wireline Receiver



隊伍名稱｜眼前一亮 Eye Opener

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研究領域

無線與有線通訊積體電路、混合信號積體電路、雷達感測系統。

作品摘要

隨著人工智慧、高效能運算及雲端資料中心的快速發展，超高速有線傳輸技術已成為次世代通訊系統的關鍵核心。為滿足 112/224 Gb/s 高速 SerDes 的傳輸需求，接收端必須克服長距離通道所造成的高頻損耗、符際干擾(ISI)及雜訊增加等挑戰。當傳輸速率提升至 224 Gb/s 時，通道於奈奎斯特頻率下的插入損耗可能超過 35 dB，使傳統類比等化器在功耗、調整彈性及效能表現上面臨顯著限制。本作品針對採用類比數位轉換器(ADC)之高速接收機，提出一套適用於 112/224 Gb/s 超高速有線通訊之數位訊號處理器 (DSP)架構，藉由高速數位等化與自適應演算法，提升整體訊號品質與傳輸可靠度。

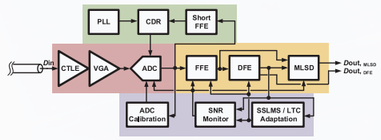
本作品展示一套 160 路平行化 DSP 架構，支援 224 Gb/s 超高速資料吞吐量，並兼顧數位電路之時脈限制，同時針對等化器與電路模組進行架構創新與效能最佳化設計。 核心電路包含前饋式等化器(FFE)、決策回授等化器(DFE)、最大概似序列檢測器(MLSD)，以及背景式資源重配置機制(SNR Monitor)。

在前饋式等化器方面，結合自動化設計流程、快速 FIR 演算法及平行化展開技術，可自動產生適用於不同平行化架構之高效能電路設計。在決策回授等化器方面，結合滑塊式架構與前饋等化種子碼技術，於解碼前先對種子碼進行額外等化，解決傳統滑塊式架構於高損耗環境下保留過多歷史解碼資訊而導致的時序違規與複雜繞線問題。

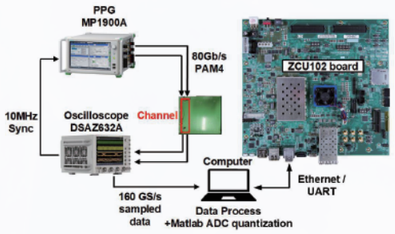
在最大概似序列檢測器(MLSD)方面，本研究提出以決策回授等化器(DFE)為基底之區域檢測架構，結合降維狀態技術，實現低複雜度設計，在顯著降低硬體面積與功耗的同時，仍可維持全狀態檢測器優異之誤碼率表現。

除等化與解碼器外，本研究亦導入背景式訊雜比監測與資源重配置機制，可根據通道品質即時啟用或關閉部分電路模組，以降低系統功耗。整體系統以FPGA 展示並以台積電 16 奈米 CMOS 製程實現，結合類比前端可支援超過 35 dB 通道損耗環境，並達成前向錯誤修正前(pre-FEC)誤碼率低於10^{-6}之設計目標。

本研究成果可應用於人工智慧資料中心、高速網路交換器、矽光通訊及次世代高速傳輸晶片等領域，極具未來高速與低功耗 SerDes的應用價值與發展潛力。



圖一 接收機系統架構圖。



圖二 數位訊號處理器之FPGA量測環境架設。

Abstract

Driven by the rapid growth of artificial intelligence (AI), high-performance computing (HPC), and cloud-scale data centers, ultra-high-speed data links have become the critical backbone of next-generation communication systems. To support 112 Gb/s and 224 Gb/s data Serializer/Deserializer (SerDes) architectures, high-speed receivers must overcome severe signal integrity challenges, including high-frequency channel loss, inter-symbol interference (ISI), and noise amplifications. At 224 Gb/s operation, channel loss at the Nyquist frequency can exceed 35 dB. It drastically limits the performance of conventional analog equalizers in terms of power efficiency, flexibility, and scalability.

To address these challenges, this work proposes a Digital Signal Processing (DSP) solution for 112/224 Gb/s ADC-based ultra-high-speed wireline receivers. The proposed architecture enhances signal quality and transmission reliability through high-speed digital equalization and adaptive signal processing techniques.

To support 224 Gb/s data throughput under stringent timing constraints of digital circuits, a 160-way parallel DSP engine is presented, featuring an innovative system architecture and optimized submodule designs. The core circuits integrate a Feed-Forward Equalizer (FFE), a Decision Feedback Equalizer (DFE), a Maximum Likelihood Sequence Detector (MLSD), and a background Signal-to-Noise Ratio (SNR) monitor for dynamic hardware reconfiguration.

For the FFE, an automated design agent supporting both fast FIR algorithm (FFA) and parallel unrolling technique is deployed. This framework automatically generates highly efficient circuits tailored to various input and output parallelism configurations. The DFE design adopts a sliding-block architecture incorporating a feed-forward seed pre-equalization. This approach resolves the critical long-history-block bottleneck inherent in conventional architectures, thereby circumventing timing violations and routing congestion under severe channel-loss conditions.

For the MLSD design, a DFE-based region detector is proposed for reduced-state trellis pruning. It significantly reduces hardware complexity and power consumption while maintaining comparable Bit Error Rate (BER) performance as that of a full-state MLSD.

In addition, a background SNR monitor enabling dynamic hardware reconfiguration is proposed. Based on the real channel conditions, specific hardware cores such as filter-taps can be partially powered down to further enhance energy efficiency. The proposed DSP engine was verified on an FPGA platform and implemented in a TSMC 16 nm CMOS process.

With an integrated analog front-end (AFE), the receiver can compensate up to 35 dB channel loss at the Nyquist frequency, achieving a pre-forward error correction (pre-FEC) Bit Error Rate (BER) below 10^{-6}.

The proposed architecture is highly applicable to next generation high-speed transceiver ASICs, silicon photonics (co-packaged optics), and high-speed network switches in AI data centers. It demonstrates strong competitive potential for future high speed, low power Serdes applications.

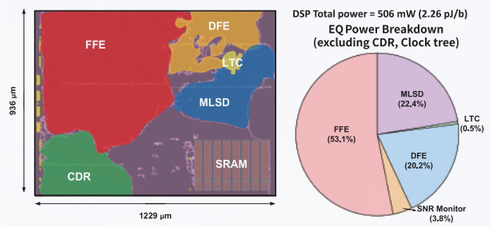


Fig. 3 DSP post-layout and power break down.

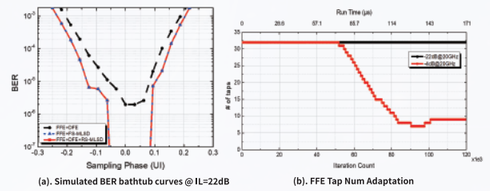


Fig. 4 (a) Bathtub curve@22dB IL. (b) Resource configuration measurements of FFT taps number under different channels.