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適用於下世代6G應用之95.3%高效率多模式多頻段封包追蹤發射機

A Multimode Multiband Envelope-Tracking Transmitter Achieving 95.3% Efficiency for Next-Generation 6G Applications



隊伍名稱｜洋青椒好難配隊
Green Peppers Are Hard to Pair

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臺灣大學電機工程學士、碩士、博士，現為陽明交通大學電機工程學系講座教授以及IEEE Fellow。曾於1996至1998年任臺北飛利浦公司兼職IC設計人員，1998至2000年任Avanti擔任項目經理，從事電源管理IC的設計。成立陽明交通大學混合信號和電源管理IC實驗室，在IEEE頂尖期刊(JSSC及TPE)和會議(ISSCC及VLSI symposium)上有卓越的貢獻，並擁有多項專利。

研究領域

電源管理積體電路設計、混合訊號電路設計、液晶顯示器（LCD）驅動器設計、氮化鎵驅動器設計。

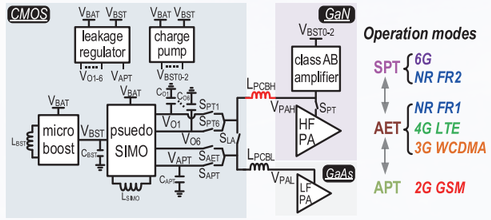
作品摘要

隨著無線通訊系統從早期單載波標準逐步演進至5G NR的先進多載波架構，發射訊號的峰均功率比(PAPR)持續提高，使功率放大器(PA)在功率回退區面臨嚴重效率衰減，傳統固定電壓供應方式無法隨訊號封包變化調整供應電壓，導致多餘能量以熱的形式耗散，限制其在現代與未來通訊系統中的適用性，因此動態電源供應調變成為提升PA效率的重要技術，其中封包追蹤(Envelope Tracking，ET)可依據訊號功率變化即時調整PA供應電壓，以降低高PAPR所造成的效率損失。

然而不同ET方法如平均功率追蹤(APT)、類比封包追蹤(AET)、數位封包追蹤(DET)與符元功率追蹤(SPT)，各自在效率、頻寬、線性度與電路複雜度之間存在權衡，同時多模多頻PA的操作需求與PCB寄生電感所引發的電壓振盪，也進一步增加高效能、可擴充ET系統的設計難度，本作品透過CMOS、GaN與GaAs組成的三晶片架構，兼顧成本、效率、高頻能力與多頻段相容性，CMOS晶片負責實現偽單電感多輸出轉換器、微型升壓轉換器、電荷幫浦與漏電調節器，提供高效率且可快速切換的電源調變，GaN晶片整合高頻PA與純空乏型三級AB類放大器，利用GaN在高頻、高功率密度與高效率上的優勢支援5G FR2與未來6G操作，GaAs模組則支援低頻多模多頻PA，使系統可涵蓋2G至5G FR1應用。

為因應不同通訊標準與頻寬需求，本系統支援APT、AET與SPT 三種操作模式，APT適用於低頻寬2G場景，AET用於3G、4G與5G FR1，以混合式電源調變兼顧效率與線性度，SPT則面向5G FR2與6G高頻寬應用，透過符元級供應電壓調整提升效率並放寬類比追蹤頻寬限制，此外本作品利用GaN三級AB類放大器作為主動式緩衝器，有效抑制因PCB寄生電感與PA去耦電容形成高品質因子諧振網路所造成的VPA電壓振盪，避免額外LC濾波器帶來的面積與複雜度問題。

實驗結果顯示，所提出架構在SPT模式下峰值電源調變效率可達95.3%，並具備寬頻、快速切換與高穩健性的特點，確保在不斷演進的通訊標準下都能擁有無縫的性能表現，展現次世代6G無線系統的實用可行性潛力。



圖一 ETSM發射器整體架構圖。

Abstract

As wireless communication systems have evolved from early single-carrier standards to the advanced multi-carrier architecture of 5G NR, the peak-to-average power ratio (PAPR) of transmitted signals has continued to increase, causing severe efficiency degradation in power amplifiers (PAs) under power back-off operation. Conventional fixed-voltage supply schemes cannot adjust the supply voltage according to envelope variations, resulting in excessive energy dissipation in the form of heat and limiting their applicability in modern and future communication systems. Therefore, dynamic power supply modulation has become an important technique for improving PA efficiency. Among these techniques, envelope tracking (ET) dynamically adjusts the PA supply voltage according to signal power variations, thereby reducing the efficiency loss caused by high-PAPR signals.

However, different ET approaches, such as average power tracking (APT), analog envelope tracking (AET), digital envelope tracking (DET), and symbol power tracking (SPT), involve trade-offs among efficiency, bandwidth, linearity, and circuit complexity. In addition, the operating requirements of multi-mode multi-band PAs and voltage ringing caused by PCB parasitic inductance further increase the design challenges of high-efficiency and scalable ET systems. This work adopts a three-chip architecture composed of CMOS, GaN, and GaAs technologies to balance cost, efficiency, high-frequency capability, and multi-band compatibility. The CMOS chip implements a pseudo single-inductor multi-output converter, a micro boost converter, a charge pump, and a leakage regulator, providing highly efficient and fast-switching power modulation. The GaN chip integrates a high-frequency PA and a fully depletion-mode three-stage class-AB amplifier, leveraging the advantages of GaN in high-frequency operation, high power density, and high efficiency to support 5G FR2 and future 6G applications. The GaAs module supports low-frequency multi-mode multi-band PAs, enabling system coverage from 2G to 5G FR1 applications.

To address the requirements of different communication standards and bandwidths, the proposed system supports three operation modes: APT, AET, and SPT. APT is suitable for low-bandwidth 2G scenarios, while AET is adopted for 3G, 4G, and 5G FR1 applications, achieving a balance between efficiency and linearity through hybrid power modulation. SPT targets high-bandwidth 5G FR2 and 6G applications by adjusting the supply voltage at the symbol level, improving efficiency while relaxing the bandwidth requirement of analog envelope tracking. In addition, this work employs the GaN three-stage class-AB amplifier as an active buffer to effectively suppress VPA voltage ringing caused by the high-Q resonant network formed by PCB parasitic inductance and PA decoupling capacitance, avoiding the area and complexity overhead introduced by additional LC filters.

Experimental results show that the proposed architecture achieves a peak supply modulation efficiency of 95.3% in SPT mode, while offering wide bandwidth, fast switching, and high robustness. These features ensure seamless performance under continuously evolving communication standards and demonstrate the practical feasibility of the proposed system for next-generation 6G wireless applications.

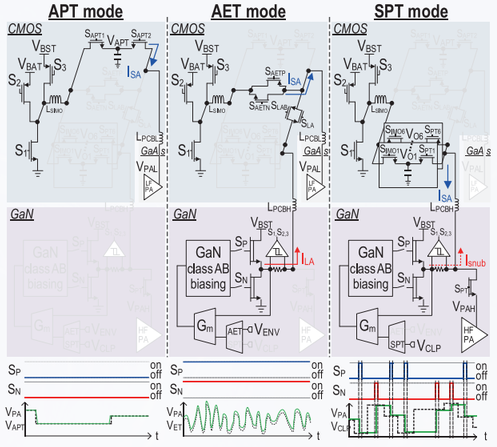


Fig. 2 Operation of the proposed ETSM in APT, AET, and SPT modes.