D26-098

# 基於標準CMOS製程之高靈敏度雙間隙超聲波單晶片系統

## A Novel High-Sensitivity Dual-Gap Ultrasound System-on-Chip Based on Standard CMOS Process




隊伍名稱｜尼的超聲波好像有點東西
Your Ultrasound Sounds Like Something

隊　　長｜許惟翔 / 清華大學奈米工程與微系統研究所

隊　　員｜陳旭中 / 清華大學動力機械工程研究所


## 指導教授 ADVISOR




### 李昇憲 | 清華大學奈米工程與微系統研究所

美國密西根大學電機博士，現為清華大學講座教授。曾擔任清華大學奈米工程與微系統研究所所長、動力機械工程學系副系主任。目前擔任國科會自動化學門召集人、科技政策諮詢專家室工程戰略群組領域專家，致力於推廣射頻微機電系統與微感測器。


### 研究領域

射頻微機械電路、共振式微感測器、單晶片系統整合。

## 作品摘要

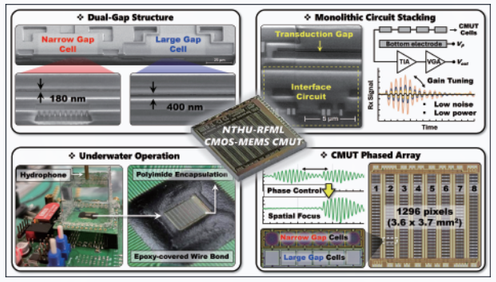

隨著物聯網、智慧醫療與非破壞性檢測技術的高速發展，市場對於微型化、低功耗且具備高解析度的超聲波感測器需求日益迫切。目前主流的超聲波換能器仍多採用壓電陶瓷，然而其聲學阻抗與水或人體組織等傳遞介質匹配度差，加上元件體積龐大、需人工組裝、以及難以與驅動電路進行高密度整合等生產劣勢，導致系統成本居高不下，同時也限制了其在穿戴式裝置與體內成像的應用。電容式微機電超聲波換能器CMUT因具備頻寬廣、靈敏度高且易於陣列化之優勢，被視為取代傳統壓電陶瓷探頭的明日之星。本作品結合標準半導體製程與獨特的後製程處理技術，提出了全球首創的「雙間隙CMUT-on-CMOS」單晶片解決方案。

我們在單一晶片上同時實現了兩種截然不同間隙的換能器陣列，如圖一所示。利用180 nm極窄間隙的MIM (Metal-Insulator-Metal)結構作為高靈敏度接收端，其低操作電壓與高機電耦合強度，使其能偵測微弱的超聲波回波；同時，利用400 nm較大間隙的TiN-C (Titanium Nitride Composite)結構作為高功率發射端，確保足夠的聲壓輸出。雙間隙設計如同在微型揚聲器/麥克風內打造兩個協同運作的共鳴腔：較小的間隙提供高靈敏接收，較大的間隙強化發射能量，在節省晶片面積的同時兼顧訊號品質以及能量效率。

不同於傳統MEMS需仰賴昂貴的客製化光罩與複雜的對準步驟，本作品利用台灣積體電路製造股份有限公司提供之標準的0.18 μm CMOS製程製作，僅需透過簡單的後段「無光罩」蝕刻技術即可完成。

我們巧妙地利用CMOS製程中既有的金屬層(Metal-3與Capacitor Top Metal，CTM)作為犧牲層，並以金屬層內氮化鈦(Titanium Nitride，TiN)抗反射層作為結構電極，成功在不改變標準設計規則的前提下，精確定義出微米級的微機電結構。此創新大幅降低了生產成本與技術門檻，極具量產潛力。

本作品成功將微機電感測器直接製作在CMOS電路的正上方，實現了真正的三維垂直整合。晶片底層整合了轉阻放大器，感測訊號可透過最短路徑傳輸至電路，降低了寄生電容與傳輸雜訊。與傳統將感測器與電路分開製造再透過打線接合的封裝方式相比，本設計在雜訊抑制上具有絕對優勢。


圖一 首創單晶片 CMOS-MEMS 雙間隙超聲波收發系統。

## Abstract


Driven by the rapid growth of the IoT, smart healthcare, and nondestructive testing, the demand for miniaturized, low-power, and high-resolution ultrasonic sensors is becoming increasingly urgent. Currently, mainstream transducers employ bulk piezoelectric ceramics. However, they suffer from poor acoustic impedance matching with media like water or tissue, bulky volumes, manual dicing assembly, and difficulties in high-density IC integration. These drawbacks lead to high costs and limit applications in wearables and in vivo imaging. Featuring a broad frequency spectrum, high sensitivity, and simplified array design, Capacitive Micromachined Ultrasonic Transducers (CMUTs) are considered as the rising stars to replace conventional probes. Combining standard semiconductor fabrication with an ingenious post-processing technique, this work proposes a groundbreaking, globally pioneering "dual-gap CMUT-on-CMOS" monolithic single-chip solution.

We have successfully implemented two distinct transducer arrays with completely different gaps on a single chip. A 180 nm narrow gap Metal-Insulator-Metal (MIM) structure serves as the highly sensitive receiving end; its low operating voltage and high electromechanical coupling capability enable the detection of weak echoes. Concurrently, a 400 nm larger gap Titanium Nitride Composite (TiN-C) structure serves as the high-power transmitting end to ensure sufficient acoustic pressure output. This dual-gap design functions like crafting two collaborative resonant cavities within a speaker/microphone system: the narrower gap provides high-sensitivity reception, while the larger gap reinforces transmission energy. This optimizes signal quality and energy efficiency while saving chip area.

Unlike conventional MEMS devices that rely on expensive custom photomasks and complex alignment steps, this work leverages the standard 0.18 μm CMOS process provided by TSMC, requiring only simple back-end maskless etching techniques for completion. We cleverly utilize existing CMOS metal layers (Metal-3 and Capacitor Top Metal, CTM) as sacrificial layers and adopt the built-in Titanium Nitride (TiN) anti-reflection coating within the metal layers as the structural electrodes. This allows us to precisely define microscale micromechanical structures without altering standard design rules, significantly reducing manufacturing costs and technical barriers while demonstrating tremendous mass production potential.

Furthermore, this work successfully fabricates the micromechanical sensors directly on top of the CMOS circuitry, achieving real vertical integration. As illustrated in Fig. 2, the bottom layer of the chip integrates a transimpedance amplifier (TIA), allowing the sensed signals to be routed to the circuitry via the shortest possible path, minimizing parasitic capacitance and transmission noise. Compared to conventional packaging approaches where the sensors and circuits are manufactured separately and connected via wire bonding, this design holds an absolute advantage in noise suppression.

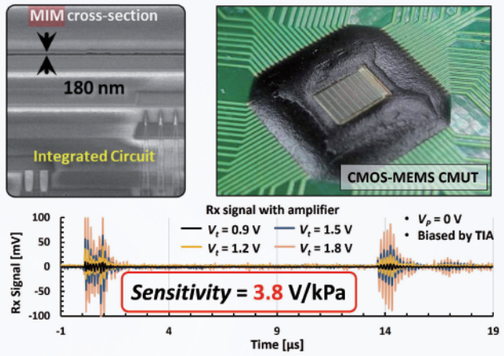




Fig. 2 Monolithic integration of CMUT and circuit achieves outstanding sensitivity.