作品名稱

應用於低功耗可攜式裝置使用3D堆疊憶阻器之 非揮發性靜態隨機存取記憶體

A Low Store Energy, Fast Power On/Off 3D-Stacked

Memristor-based Nonvolatile SRAM for Low **Power Mobile Applications**

隊伍名稱

醫龍生活 Medical Dragon Life

隊長

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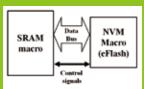
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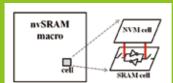
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許多可攜式裝置的系統使用雙記憶體(2-macro)的方法,揮發 性及非揮發性記憶體(例如:靜態隨機存取記憶體 + 快閃記 憶體),如Figure 1所示,來達成開機模式(active-mode)高效 能以及低電壓操作下關機(power off)時的資料儲存 (非揮發 性記憶體儲存)。然而,因在揮發性及非揮發性記憶體間的 逐字元(word-by-word)序列式資料傳輸,尤其在快閃記憶體 中,寫入需要很長的時間。使用雙記憶體架構(2-Macro)會使 得儲存和恢復時間變得很長。緩慢的儲存及恢復速度使得 可攜式系統須要提供電源很長的時間,很容易遭受到突然 斷電的傷害。

此作品提出一個以憶阻器為基礎的非揮發性靜態隨機記 憶胞(nvSRAM cell),為八個電晶體及二個憶阻器(8T2R),如 Figure 2所示。 並將其應用組成一非揮發性靜態隨機存取記 憶體(nvSRAM),來達到快速的逐位元平行儲存及恢復操作。 其消耗低儲存及恢復能量,並擁有很小的細胞面積。此8T2R nvSRAM (Rnv8T) 細胞使用二個可快速儲存的憶阻器元件,三 維堆疊於8T細胞上方,並有一個創新的二個憶阻器電晶體





開關,能夠提供憶阻器控制以及輔助靜態隨機存取記憶體 的寫入功能。此寫入輔助功能使得Rnv8T 細胞能夠使用有 利於讀取的電晶體大小,在較低的電壓下抗衕讀取失敗。 此Rnv8t作品可應用在數位電路中的閂鎖器(Latch)及暫存器 (Flip-flop)方面。

此非揮發性靜態隨機存取記憶體(nvSRAM)為第一個以憶阻 器為基礎的非揮發性記憶體晶片。已使用0.18微米製程下線 驗證成功。此16千位元Rnv8T晶片最低讀寫操作電壓為0.45

伏特,儲存耗能約為 傳統的五萬分之一: 喚回時間僅為傳統的 百分之三。在所有非 揮發性靜態隨機存取 式記憶體與二個記憶 體架構(2-Macro)中: 其儲存耗能及最低讀 寫操作電壓為最低, 如Figure 3所示。此 作品亦可應用在快速 關機,並在突發斷電 時確保系統穩定,對 電子記憶體架構可有 革命性的改變。

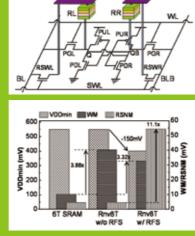


Figure 2. (a) Rnv8T structure and

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- 具備10年以上的產業界服務經驗,曾在美國New Jersey 服務於Mentor Graphics之 ICTechnology Center,回國後加入臺積電,後來於積丞科技擔任處長,專注從事矽智 產研發以及管理的工作,2006年進入清華大學電機工程學系任教至今。。
- 研究領域:記憶體電路設計,致力於高良率、低功耗、低操作電壓、3D結構之記憶 體電路研究。



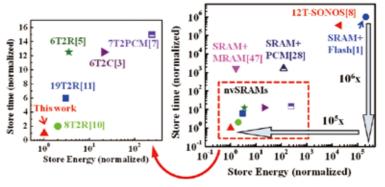
ABSTRACT

Many mobile SoC chips employ the two-macro approach, volatile and nonvolatile memory macros (i.e. SRAM + Flash), to achieve high-performance or low-voltage operation with power-off nonvolatile data storage, as shown in Figure 1. However, the "twomacro" solution suffers long store and restore time due to wordby-word serial data transfer between the volatile and nonvolatile memories. Especially, the Flash memory requires long write time. Slow store/restore speed causes a mobile system to require long power-on/off time and being vulnerable to sudden power failure.

This work proposes a memristor-based latch, a 8T2R nonvolatile SRAM (nvSRAM), to achieve fast bit-to-bit parallel store/restore op-eration, low store/restore energy, and a compact cell area. This 8T2R nvSRAM (Rnv8T) cell uses two fast-write memristor (RRAM) devices, 3D stacked over the 8T, and a novel 2T memristor-switch which pro-vides both memristor control and SRAM write-assist

functions, as shown in Figure 2(a). This write assist feature enables Rnv8T cell to use read favored transistor sizing against read/write failure at a lower VDD. This work also can be applied to the latch or flip-flop in the digital integrated circuit.

This work also demonstrates the first fabricated macro-level memristor-based nonvolatile SRAM. It is verified in the 0.18um process. This 16Kb Rnv8T macro can operate (R/W) at 0.45V VDDmin. The store energy is 1/50k times lower than conventional circuit, the restore time is simply 0.03 times as conventional one. It achieves the lowest store energy (1/50k of conventional) and R/W VDDmin (0.45V) than other nvSRAM and "SRAM+NVM" solutions, as shown in Figure 3. This work could be applied to fast power off, and ensure data stability when a suddenly power failure occurred in a system. There may be evolutionally change in the electronic memory.



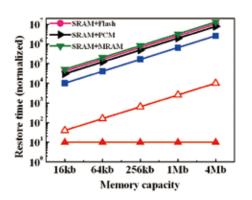


Figure 3. Comparison of (a) Store energy and (b) Restore time improved.