D11-079

作品名稱 **適用於電流引導式數位類比轉換器之無雜散動態範圍提升技術**
SFDR Enhancement Technique for Current-Steering Digital-to-Analog Converter

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作品摘要

因應高速操作，電流引導式架構是被廣泛採用的，然而，非理想的電流切換限制了無雜散動態範圍的頻寬，當輸入之數位信號達高頻時無雜散動態範圍也急速下降。為了保持良好的高頻無雜散動態範圍，本作品提出「數位式亂數歸零法」，且吾人實現一個八位元、每秒十六億個取樣之數位類比轉換器此數位類，其無雜散動態範圍優於六十分貝，直至輸入頻頻高達四點六億赫茲，功率消耗量為九十毫瓦。

當高解析度的電流引導式數位類比轉換器是必須時，電流源就得高度滿足匹配特性，其付出的代價
即為大面積且本質電容、雜散電容也變大因而導致頻寬下降，改善此現象的途徑為使用較小面積的電流源。然而，小面積電流源將引起嚴重的不匹配，本文提出一個背景校正技術來保確高精準度。

為驗証此背景校正理論，吾人實現一個十二位元轉換器。此轉換器功率消耗為一百二十八毫瓦，操作速度可達每秒十二點五億個取樣。當頻率高達五億赫茲時，此數位類比轉換器有優於七十分貝之無雜散動態範圍。

ABSTRACT

This work focuses on the Digital-to-Analog Converters (DACs). The current-steering structure has been widely used in high-speed DACs, since in this structure the main speed limitation comes from the output node, and high sampling speed is thus easily achieved. However, the non-ideal switching limits the bandwidth of spurious-free dynamic range(SFDR). The SFDR decreases rapidly with increasing input frequency. Therefore, Digital Random Return-to-Zero(DRRZ) is proposed for the high sampling rate current-steering DAC to maintain high SFDR at high frequency.

To demonstrate the proposed Digital Random Return-to-Zero technique, a CMOS 8-bit 1.6-GS/s DAC was fabricated in a 90 nm CMOS technology. The DAC achieves a SFDR better than 60 dB for a sinewave input up to 460 MHz, and better than 55 dB up to 800 MHz. The DAC consumes 90 mW of power.

In the design of high-accuracy current-steering DACs, current sources with high matching property are required and the penalty is large area. Intrinsic and parasitic capacitor loading also degrade the signal bandwidth. The way to reduce loading is using compact current cells. In this thesis, background calibration is proposed to correct the mismatch current caused by small dimension.

To verify the proposed background calibration algorithm, a 12-bit DAC was fabricated in 90nm CMOS technology and using compact current cells. The area of current sources are 1/400 of the required area which is designed for 12-bit resolution. The chip consumes 128mW. Active area is 1100umx750um. At 1.25GS/s sampling rate, the DAC achieves better SFDR than 70dB up to 500MHz input frequency.

D11-107

作品名稱 **適用於下世代手機通訊之LDPC Convolutional Code編解碼器設計**
LDPC Convolution Codec Design for Next Generation Mobile Communications

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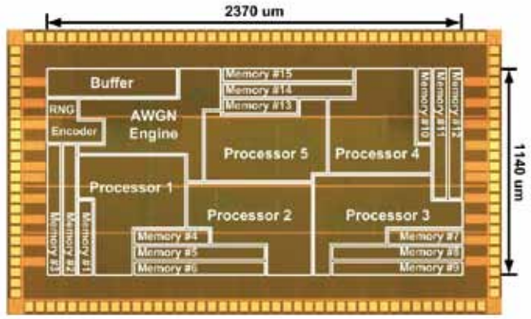
作品摘要

行動通訊系統中，通道編解碼模組往往扮演關鍵角色，不僅要達到高吞吐量的傳輸需求，也必須降低伴隨而來的功率消耗，以提供具有技術競爭力的解決方案。低密度奇偶校驗迴旋碼（LDPC convolutional codes，簡稱LDPC-CCs）於1999年提出，此碼具有彈性的碼率與區塊長度、簡單的編碼電路、較低的繞線複雜度，相較於渦輪碼（Turbo codes），更易於實現高速的吞吐量並且降低功率消耗。

據此，本作品提出演算法、節點、位元等三個層級的最佳化架構來提升吞吐量、減少硬體花費及降低解碼延遲時間，並藉由混合分割式FIFO架構來降低功率消耗。演算法層級最佳化可加速解碼收斂速度，減少一半所需的處理單元，節點層級最佳化可將平行度提高到12，並同時降低解碼延遲12倍。使用UMC 90 nm製程下線，在1.2V電壓下晶片實際量測到198 MHz，資料吞吐量高達2.37 Gbps，解碼器部分晶片面積僅佔2.24 mm2，功率消耗為284mW，能源效率為0.024 nJ/bit/proc。總言之，此作品在各方面都具有極高的競爭力，相當適合於未來使用手持行動裝置的高網路傳輸速度要求。



實作晶片圖
(包含完整的低密度奇偶校驗迴旋碼解碼器以及測試電路)

ABSTRACT

In mobile communication system, channel coding modules used to play an important role. To provide a highly competitive solution, reaching high data-transmission rate is required, so does reducing the high power consumption. Low-Density Parity-Check Convolutional Codes (LDPC-CCs) were introduced in 1999, which possess flexible code-rates, variable length of data frame, simple encoding circuitry, and low routing complexity. Compared to the Turbo decoder, the LDPC-CC decoder is more suitable for highly-parallel implementation and low-power architecture.

Therefore, our work proposed three level optimization techniques, including algorithm-level, node-level and bit-level, to increase decoding throughput, lessen hardware costs, and reduce decoding latency. Moreover, a hybrid-partitioned FIFO structure is presented to further reduce power consumption. The algorithm-level optimization accelerates the decoding convergence, which leads to the result that only half number of processors is required under the same BER performance. The node-level optimization can increase the parallelism to 12, and reduce 12 times of the decoding latency concurrently. Fabricated in UMC 90nm 1P9M CMOS process, the proposed LDPC-CC decoder chip could achieve maximum 2.37Gbps under 198 MHz operating frequency. The decoder containing 5 processors only occupies an area of 2.24 mm2 and draws 284mW with an energy efficiency of 0.024 nJ/bit/proc. In conclusions, our proposed LDPC-CC decoder outperforms state-of-the-art designs and is suitable for the high-speed transmission requirements of next-generation handheld mobile devices.