D11-108

作品名稱 **應用於連續醫療照護之低耗能無石英晶體基頻收發器設計**
An Energy-Efficient Crystal-less Baseband Transceiver for Continuous Healthcare Applications

隊伍名稱 **1479王朝 Dynasty of 1479**
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作品摘要

作品呈現一無石英震盪器和極低能源消耗之無線收發晶片組，以滿足低耗能、微型化、低成本、高可靠度傳輸之長期連續醫療看護需求。

對於資訊量較低的無線生理訊號監控，前端射頻電路消耗功率佔全系統 80% 以上，最有效降低能量使用率的方式是讓系統長時間以極低的速度處理和儲存生理訊號，等訊號累積至一定容量後再以較高的傳輸速率在極短時間內傳送，減少前端電路的開啟時間。為滿足傳輸可靠度和較高速的傳輸速率，我們採用正交分頻多工的調變技術。為進一步降低前端電路能量消耗，我們使用一均峰值壓縮器將訊號振幅上的變化轉換成相位的變化傳送，改善功率放大器的轉換效率。同時，也加入迴旋碼通道編碼改善錯誤率紓減傳輸所需的功率。

最後，我們以矽震盪器取代石英晶體來提高整合度和實現微型化。在頻率精準度上，矽震盪器擁有將製程-電壓-溫度變異所導致的頻率偏移作自我校正能力，並藉由時脈追蹤校正電路做細調，讓系統頻率準確度滿足高速傳輸的需求。

ABSTRACT

This work presents an energy-efficient crystal-less baseband transceiver for continuous healthcare monitoring. The proposed system enables low-energy, low-cost reliable transmission with miniature integration factor.

For low information rate application, the RF front-end circuits consume 80% system power in active mode. The most energy-efficient way is storing the body signal in most time. Then, the data is transmitted through a high data rate link in a bust duration to minimize the RF operation time. So, the orthogonal frequency division multiplexing modulation scheme is applied to provide higher throughput and reliable transmission at the same time. To further reduce the front-end power, the peak-to-average power ratio compressor and convolutional coding are applied to suppress the signal PAPR and transmitted power level.

On the other hand, for miniature form factor, an on-chip CMOS oscillator is integrated to replace the use of quartz crystal. A process-voltage-temperature calibrator is applied to perform initial coarse frequency tuning. Then, a clock recovery loop provides the final convergence accuracy compatible with our target system throughput.

D11-115

作品名稱 **一個三維晶片高速效能自我測試使用之雙緣夾擊技術**
A High-Performance Self Test Using Double Edge Clipping Technique for 3D Chip

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作品摘要

目前的電路延遲測試是使用測試機台(Automation Test Equipment；ATE)來測試，但由於電路的低電壓設計及雜訊電壓等所引起的待測電路發生延遲，都造成使用ATE或掃描測試技術均難以正確擷取電路輸出端的延遲時序，因此本論文提出一內嵌式電路延遲自我測試Delay BIST之方法。我們所設計Delay BIST電路可以達到的效果有(1)輔助待測電路(CUT)能夠被高速進行電路延遲測試(2)經由雙緣夾擊可以量測到CUT的最高工作頻率(3)數位控制脈衝波產生器(Digital Controlled Pulse Generator ；DCPG)的粗調跟細調控制信號提供高解析度量測。本設計使用TSMC 0.18 um 1P6M的製程完成晶片下線，並且結合低速測試機台驗證我們所提的方法可使用於測試高速電路，現行低速機台將可以藉由這種設計來銜接延伸裝置來測試高速電路，讓現行的低速測試機台可繼續沿用。

ABSTRACT

The testing of system design integrated circuit is highly complex. There are many test challenges generated from at-speed delay testing requirements. BIST circuit can help to solve traditionally slower ATE tester problems. In this research, a double edge clipping technique is proposed for at-speed BIST testing. It differs from traditional circuit delay testing techniques by changing the clock rate using external ATE. This method uses lower-speed input clock frequency, then applies internal BIST circuit to adjust clock edges for circuit high-speed delay testing. Test chips are fully validated. The post-layout simulations show that the wide-range (36%~74%), fine-scale (14.3ps), coarse-sacle(334ps) duty cycle adjustment technique with high-precision calibration circuit is effective for at-speed delay testing and performance binning.