Design Group D11-088

作品名稱

它抓得住我：
用於高解析度攝影機之可程式化前景偵測處理器
A programmable foreground detection processor for HD surveillance camera

隊伍名稱

追蹤者 Tracker

隊長

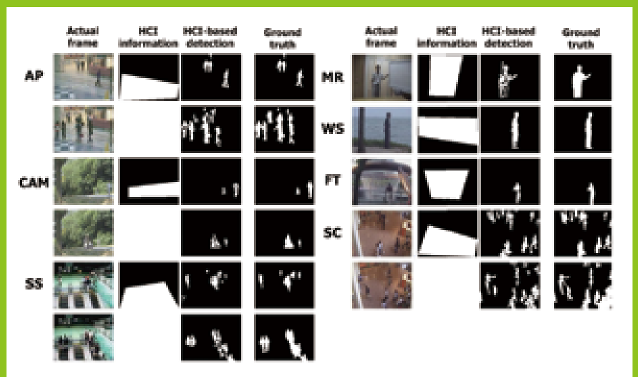
李思彥　中央大學電機工程學系碩士班

隊員

林崇元　中央大學電機工程學系博士班

作品摘要

賦予監控攝影機智慧即為我們此項作品的目標，利用電腦視覺演算法偵測、追蹤、辨識前景物件，並以這些資訊來自動偵測畫面中是否有必須注意的事件發生。我們這次的參賽作品，即為設計可用於高解析度攝影機之可程式化前景偵測處理器。在考量監控系統的成本下，最根本的作法即是將前景偵測的功能散佈到每一台攝影機當中，形成所謂的分散式智慧型監控系統，每一台攝影機必須搭載具有前景物件偵測功能的硬體。然而，前景偵測演算法多涉及下列的硬體實現瓶頸： 1. 儲存複數張背景模型，需要龐大的記憶及記憶體頻寬體需求。 2. 高解析度畫面和涉及浮點數的機率運算，造成的硬體面積以及運算時間的消耗。 3. 畫面複雜度，現實中存在許多會動的背景，包括光影的變化，風吹而搖曳的樹木，天候的改變，如下雨天，這些因素會造成前景偵測品質下降。 我們的創作動機為：融合之前開發的前景偵測演算法、用於背景維持的演算法及其硬體設計、前景物件標籤化演算法及其硬體設計等三項成果，採用軟硬體共同處理之設計準則，及Hardware/Software Co-processing，來整合上述的軟硬體成果。所實現的硬體呈現了System on Chip的架構設計，其包含了： 1. 規律資料流路徑單元 2. 低複雜度的簡單指令集處理器單元 3. 可使用者規劃之匯流排控制單元 4. 記憶體單元：此部分包括畫面及處理資料的儲存區段，以及使用者規劃程式的儲存區段 根據我們所設計的硬體，使用者可以自行規劃攝影機在前景偵測上所欲達成的功能，其包括： 1. 產生前景物件的訊息（質心、輪廓、周圍的特徵點），並將前景物件包裝成為一連續記憶體的區段存取(Foreground package)。 2. 以前景物件的面積大小對前景進行過濾。 3. 規劃畫面中感興趣的偵測區域。如Fig 1所示。 4. 規劃前景物件的追蹤，於處理器單元具有額外的運算能力。 搭載我們所設計之前景物件處理器的監控器，除了能滿足高解析度畫面所需要的即時處理能力外，背景變化的問題，如天氣、光影的變化、或是因風吹動而搖曳的樹木花草等，皆能克服並達到可容許的錯誤率。



圖一 智慧型監控攝影機之架構圖

指導教授

蔡宗漢　中央大學電機工程學系

- 蔡宗漢教授分別於1990年、1994年與1998年於臺灣大學電機系所取得學士、碩士與博士學位。
- 2000年進入中央大學電機系擔任助理教授，2004年升任副教授，2008年至今為中央大學電機工程系教授。
- 專長領域為VLSI電路設計、SOC系統設計、多媒體數位訊號處理、視訊與音訊編碼、生醫信號處理。

ABSTRACT

In this paper, the hardware-oriented technique that is based on human-machine interaction in object level (HCIiOL) is utilized to detect foreground objects with dynamic backgrounds. The proposed technique is semi-supervised which restrict the conditions for the moving object to be judge as the foreground object. The condition here is depending on background environment and is setting by HCIiOL manner. The main idea of the HMIioL is that each area should accompany different probability. The HCIiOL separates a scene of video sequence into regions by human knowledge and each region associates with different context of background object motion. Therefore, the proposed approach can provide precise foreground detection result with dynamic backgrounds and is very computational efficiency. Since the regions in the scene have been separated by the background context, our algorithm can relax/strain the restriction on pixel to be declared as foreground. The relaxing or straining restriction is adapted to the context of background object motion and can be self-trained using the multiple background maintenance (MBM) algorithms. The MBM employs the MoG model for constructing the statistical representation of the background, but different at the procedures on the update of the MoG model, background model. The foreground can therefore be detected that deviate from such model.

An example is shown in Fig. 2b in which a scene is partitioned into three areas. Area 1 contains several waving trees in the farther side of the scene. By the user knowledge, the moving object appeared in this area must have high probability for belonging to background. In comparison with area 1, the area 2 must have low probability for belonging to background object since the area contains a road in which foreground objects will pass. Therefore, the erroneous detection in area associated with dynamic background motions can be alleviated by adapting the decision threshold value to the constraint in the area.

The SoC architecture is presented as a low cost solution for the realization of the HCIiOL-based foreground detection approach. The presented SoC architecture consists of foreground detection accelerator and object level analysis accelerator for speeding up the computation-intensive operations in our algorithm, and a programmable processor for human-machine interaction and control-intensive operations in our algorithm. The area filter and connected component analysis (C. C. A.) accelerators for the computation-intensive procedures as shown in Fig. 2. Pipelining and parallelizing techniques are used to increase the throughput of the hardware. The statistical coding technique is adopted as embedded compression technique for reduction of memory bandwidth on specific data transfer.

The hardware-oriented technique that is based on human-machine interaction in object level (HCIiOL) is utilized to detect foreground objects with dynamic backgrounds. The total gate count is 88.458K, the total cell area is 653232 mm2 and the operation frequency for real-time HD720p sized sequence processing is 31.7 MHz and 300MHz for accelerators and OR1200 RISC processor respectively.

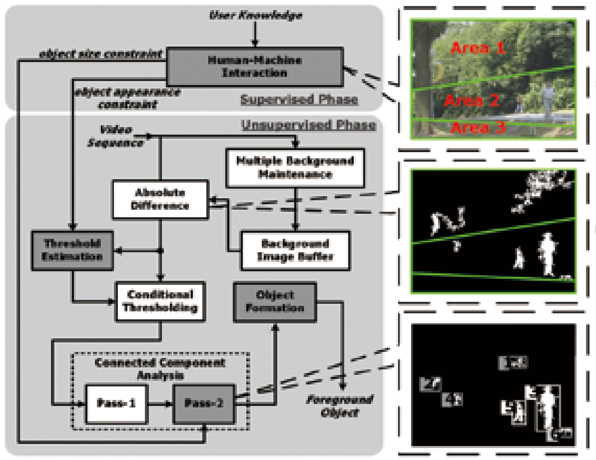


Fig.2 The result of HCIiOL