application group

AP-005

作品名稱

CMOS感測器陣列之高速攝影系統

High-Speed Videography System using Multiple CMOS Sensors

隊伍名稱

蜻蜓 Dragonfly

隊　　長

施尚君 台灣科技大學電子工程研究所

隊　　員

蔡昇達、陳首元 台灣科技大學電子工程研究所

作品摘要

高速攝影機雖然能夠為科學研究提供非常有價值的影像資料，但不論是採用CCD還是CMOS的高速感光元件，高速攝影機的價格還是普遍過高，以國外製造每秒可拍1000張的機種來說，其價格就大約要價1萬至10萬美元不等，因此我們希望能夠以多組CMOS感測器搭配SoPC的架構來實作出成本較低的高速攝影系統。

相機陣列式的攝影系統事實上是由美國史丹佛大學的計算機圖形實驗室所發展出來的，稱為「史丹佛相機陣列計畫」。在這個計畫中，他們使用了100台以上的自製CMOS相機，每組相機皆搭配了一個影像資料處理平台，其中包括了中央處理器、MPEG2編碼器、FPGA與IEEE1394等硬體以壓縮並傳送大量的影像資料至PC端，而PC端則是由四台桌上型電腦所組成。

由於上述的史丹佛相機陣列架構太過於龐大，並不適合實際應用，因此我們希望能以SoPC的架構來實作並縮減史丹佛相機陣列，如此一來勢必能讓整個系統的成本更加便宜，此外還能夠將體積大幅縮小以方便攜帶，若未來有機會將此系統產品化，想必會在原本高單價的高速攝影機市場中受到重視。

使用SoPC架構的好處是能夠輕易的將多顆CMOS感測器及各類型的控制器、編碼器等硬體整合至單一的系統平台中，而我們所使用的SoPC開發平台為友晶科技所設計的DE2發展板，其中主要有一顆Altera Cyclone II系列的FPGA晶片，用來整合Altera公司所開發的NIOS2處理器及各類型的控制器及編碼器等。另外在CMOS感測器方面，我們採用的是價格較低廉的Micron MT9M011 CMOS感測器。在軟體平台部分，為了能夠有效率且有架構的開發驅動程式與應用程式，我們決定以Linux系統來建立軟體平台。有了Linux系統所提供的豐富支援，在撰寫驅動程式時，只要遵循Linux核心中特定類型之驅動模型所提供的實作方法，便能將驅動程式的複雜度大大的降低，且在應用程式的開發上，也能有完整的函式庫支援。

由於高速攝影機每秒輸出的資料量相當大，以DE2發展板內建的8MB SDRAM根本不敷使用，因此我們打算利用發展板上的外部I/O接腳來外接了一顆32MB SDRAM。但如此一來，外部I/O接腳將被大量佔用，因此會導致在目前的DE2發展板上，剩餘的I/O接腳數只能再接2組CMOS相機。儘管如此，我們在各種軟硬體的設計上還是會以能夠連接多組CMOS相機作為前提來進行設計，以免架構過於死板而導致未來硬體擴充後軟硬體修改的難度提高。從目前硬體的規格來看，若每組CMOS相機皆能以60 fps的速度進行拍攝，我們所設計的系統將能夠提供120 fps的拍攝速度。

指導教授

許孟超 老師 台灣科技大學電子工程系所

Mon-Chau Shie (S'94 – M'98) was born in NaTou County, Taiwan, R.O.C..
He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1983, 1985, and 2000, respectively.
In fall 1988, he joined the faculty of National Taiwan University of Science and Technology, Taipei, Taiwan, R.O.C., where he is currently an Assistant Professor in the Electronic Engineering Department.
His research interests include computer architecture, embedded system, VLSI, and image compression.

Abstract

High speed video camera can provide useful and valuable image data for scientific research. But the price is the most significant disadvantage of high speed video camera. Hence we attempt to use multiple CMOS sensors and SoPC Architecture to implement a low-cost high speed video system.

Actually, the Stanford Computer Graphic Laboratory have developed "Stanford Multiple Camera Array" architecture and provided a good result in high-speed videography application. In this project, they use more than 100 CMOS cameras and every camera has its own image processing platform which includes CPU, MPEG2 encoder, FPGA and IEEE1394. The platform will transmit data to server which is the combination of four desktops.

However, the scale of the hardware architecture in their design is too large to be implemented as a portable device. Therefore, in order to reduce the architecture, we decided to realize the system with an embedded platform.

We also have developed our algorithm to do image rectification which is not mentioned in the Stanford project but is crucial to the quality of camera array. The proposed algorithms are for the most part of auto-exposure and displacement error rectification, and they are designed not only for the accurate rectifying result, the speed will be another key consideration for rectification.

The advantage of using SoPC architecture is that can easily integrate all controllers and encoders into a single integrated platform. We use DE2 development board designed by Terasic Technologies as our development platform. DE2-board includes an Altera Cyclone II series FPGA chip which is used to integrate all controllers and encoders. We also use low-cost Micron MT9M011 CMOS sensor as our video sensors. In the other hand of software, in order to design drivers and applicants efficiently, we choice uCLinux for NIOS II as our software platform. With the support of uCLinux, we can easily design drivers and applicants by following the rules of Linux driver model and by using the library provided by Linux.

Because the data of High speed video camera are very large, 8MB SDRAM on DE2-board is not enough to use. We connect another 32MB SDRAM to the expansion headers on DE2-board, and thus the remainder pins are just enough to connect 2 CMOS sensors. But our design is not limited to only two cameras. In fact, it can connect multiple CMOS sensors under the consideration of expanding hardware in the future. Now every camera can take 60 frames per second, our design has the capacity of taking 120 frames per second.