設計組 DESIGN GROUP

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作品名稱

一操作於3-10 GHz，14個頻帶並具有突波衰減功能之頻率合成器應用於超寬頻多頻帶正交分頻多工系統

A 3-10 GHz, 14-Band CMOS Frequency Synthesizer with Spurs Reduction for MB-OFDM UWB System

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作品摘要

隨著高傳輸速率無線通訊的需求，超寬頻系統被開發應用於消費性電子。其可應用於無線USB傳輸或高解析度之影像傳輸。超寬頻系統能夠擁有較高的通道容量，而因此可應用於傳輸數速率需求較高的無線個人區域網路空間。美國聯邦通訊委員會於西元2002年開放3.1-10.6 GHz之頻譜並超過500 MHz之頻帶發射之功率頻譜密度不超過41.25 dBm/MHz。

隨著多頻帶正交分頻多工系統應用於3~10GHz之超寬頻通訊系統，此規格將7GHz頻寬分割成14個528MHz之頻帶並區分為5個團體。為了要使128點正交分頻多工系統操作在高達480Mbps資料傳輸量下，其系統只允許小於9.5ns之載波頻率跳頻時間。這使得收發器晶片中之頻率合成器設計面臨兩大挑戰，一為3~10GHz之超寬頻帶操作且必須提共正交信號輸出，另一項挑戰則為小於9.5 ns之跳頻速度。

為了要符合系統嚴苛之跳頻要求（<9.5 ns），目前的研究皆朝向使用直接頻率合成技巧。然而，目前採用這方式實現之電路架構中，不是需要數個鎖相迴路，就是需要除數難以設計之除頻器，去產生適當之諧波頻率提供給系統做全頻帶之頻率合成。而目前唯一能產生全部14個頻帶之前作，卻需要串接3級之單旁帶混波器於信號路徑中。因此它們將遭遇到頻帶內之諧波失真、諧波拉扯和難以產生正交輸出信號等問題。

本設計與前作相比，我們提出了一操作於3-10 GHz，14個頻帶並具有突波衰減功能之頻率合成器，其架構將基於單一個鎖相迴路之架構。隨著適當的頻率規劃，此架構只需要鎖相迴路之迴授路徑中除2除頻器電路。因此，其可產生較精準之正交相位諧波頻率，以能讓單旁帶混波器能有更好的混頻效能。並且，串接單旁帶混波器之個數也縮減為2級，在全部14個頻帶之情形下。另外，隨著本架構中提出諧波頻率之正交信號校正功能，其鏡像突波能壓抑至40 dBc以下，並且全部14個載波頻率輸出之突波動態範圍表現可超過30 dB。

指導教授

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Abstract

THE prospect of wireless data transmission at rates of hundreds of Mbps has ignited the interest of consumer electronics in ultra-wideband (UWB) systems. Examples of possible applications include wireless USB and high-definition video streaming. Ultra-wideband (UWB) achieves a high channel capacity and hence becomes an attractive solution to the ever-increasing data rate demands in the space of wireless personal area networks (WPAN). The FCC regulations released in 2002 establish that UWB devices for communication applications can operate in the unlicensed spectrum of 3.1–10.6 GHz while employing at least 500 MHz of bandwidth (measured at the frequency points where the PSD has decreased by 10 dB) with a PSD of less than 41.25 dBm/MHz.

As proposed by MB-OFDM (multi-band orthogonal frequency division multiplexing) alliance, the spectrum for UWB communication system ranges from 3.1-10.6 GHz, which is divided into 14 bands with each band of 528 MHz and categorized into 5 groups. To meet the stringent frequency hopping time requirement (< 9.5 ns), several frequency synthesizers based on single-side band (SSB) frequency mixing are proposed recently. Nevertheless, these architectures demand multiple phase locked loops or sophisticated dividers to provide adequate sub-harmonics for the full band frequency synthesis. The only one capable of covering 14-band carrier generation in the literature requires 3 stage cascaded SSB mixers in the signal chain. As a consequence, they are susceptible to in-band spurs generation, harmonic pulling, and encounter difficulties in I/Q carrier generation.

In contrast to the prior arts, this paper proposes a 14-band, I/Q phases, CMOS frequency synthesizer based on single phase-locked loop architecture. With adequate frequency planning, only divide-by 2 dividers are needed in the feedback path of the PLL. Thus, more precisely in phase and quadrature phase (I/Q) sub-harmonics can be derived from the divider chain by nature for SSB frequency mixing. On the other hand, the number of mixer stage in cascade is reduced to 2 for full-band carrier generation. With the aid of sub-harmonic I/Q calibration, the image spurs are suppressed below –40 dBc and more than 30 dB spurious free dynamic range is achieved for the full band generation.