DESIGN GROUP 設計組

D9-091

作品名稱	降低不匹配敏感度之電容交換型循環式類比數位轉換技術 Capacitor-Swapping Cyclic A/D Conversion Techniques with Reduced Mismatch Sensitivity
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作品摘要

本作品對循環式類比數位轉換器提出隨機回授電容互換 (RFCI) 技術以及平均隨機回授電容互換 (ARFCI) 技術兩項電容交換型技術，其可藉由簡易的操作減小由電容不匹配造成的諧波失真。這兩項技術於電路實現上只需簡單的控制電路在不同的操作循環時重新配置電容連接，不需要額外大量數位電路。RFCI技術可改善傳統循環式類比數位轉換器的無雜訊動態範圍 (SFDR) 而不會犧牲信號對雜訊失真比 (SNDR)。ARFCI技術可進一步得到相對於RFCI技術更好的SNDR特性，但其SFDR的改善則較小且轉換速度略低。這兩項提出的技術可減輕轉換器在高規格的SFDR時所需之電容匹配需求，因此設計上電容值可縮減至符合SNDR的要求，而可減少運算放大器所需的推動能力，也因而使轉換器整體功耗及面積減少。先前已被提出之交替回授電容切換 (CFCS) 技術雖然對SFDR較無功效，但可改善信號雜訊比 (SNR)。本作品亦提出中一個可重新配置的循環式類比數位轉換器架構，用一個簡單的時序控制電路就能夠很容易地重新配置轉換器使其操作於RFCI、ARFCI、CFCS三個技術的其中之一。本作品以MATLAB驗證比較所提技術之效果，並且使用0.35um 2P4M 3.3V CMOS製程設計一個單晶片實作。此晶片大小尺寸為0.83 mm × 0.76 mm。經由量測亦驗證了本作品提出的技術與架構確可被實現來改善循環式類比數位轉換器的效能。

Abstract

This work proposes two capacitor-swapping techniques, random feedback-capacitor interchanging (RFCI) and averaging RFCI (ARFCI) techniques, for cyclic analog-to-digital converters (ADCs) to reduce the harmonic distortion caused by capacitor mismatch. The proposed RFCI and ARFCI techniques can be realized by rearranging the capacitor connections of the ADCs in different operation cycles with simple circuits. The RFCI technique improves upon the spurious-free dynamic range (SFDR) of conventional ADCs without sacrificing the signal-to-noise-and-distortion ratio (SNDR). The ARFCI technique has better SNDR characteristics but less SFDR improvement than RFCI. With RFCI and ARFCI, the capacitor matching requirement is relaxed for high SFDR and the capacitance can then be reduced to meet the SNDR requirement, reducing the driving capability of the opamps, and thus reducing the total power and area of the ADCs. The prior commutated feedback-capacitor switching (CFCS) technique has less effect on the SFDR of cyclic ADCs but improves the signal-to-noise ratio (SNR). This work proposes a reconfigurable cyclic ADC architecture that can be easily reconfigured to operate with one of the RFCI, ARFCI, and CFCS techniques by a simple timing control circuit. MATLAB simulations and a chip implementation are employed in this work to demonstrate the proposed approaches.