D10-042

作品名稱

應用於低功耗可攜式裝置之超低電壓反及閘型唯讀記憶體

An Ultra Low Voltage Embedded NAND-ROM for Low-Power Portable Electronics

隊伍名稱

咱丟係愛地球 We love the Earth

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作品摘要

近年來，低功率消耗的應用越來越被重視，如感測網絡、生醫電子、航太科技與低功耗可攜式電子產品等等，超低電壓的操作為延長電池壽命最有效的方法之一。許多內嵌式系統需要大容量的唯讀記憶體儲存系統程式與資料，唯讀記憶體具備小尺寸、高可靠度、低成本、低功率消耗等特性，是常見系統晶片中不可或缺的基礎功能區塊。反及閘型的低漏電流特性適用於長時間處於待機狀態的低電壓系統晶片應用中是大容量、低功耗應用較好的選擇。

因製程微縮，金屬線之間的距離減小導致嚴重的耦合干擾效應，在傳統的反及閘型唯讀記憶體中，這些耦合的雜訊、電荷分享效應及位元線漏電流會導致讀1錯誤的情況。為了避免此情況，通常會降低讀取參考電壓，但由於製程變異造成細胞電流分佈大，需要較大的讀0感測邊界，因此讀0錯誤的情況會更為嚴重。所以我們利用動態源極充放電路將奇數與偶數的源極線分開，在讀取時，非選取的源極線將保持在高電位以作為相臨位元線之屏障，可使選取到的位元線不受耦合雜訊干擾，同時也消除非選取位元線的漏電流，以避免讀1錯誤的情況。另外，偵測參考電位產生電路能提供回授至讀取參考電位，當偵測出讀取資料為0時，回授電路會提高參考電位，以此方式放大感測邊界。為了達到更低的操作電壓，我們提出資料處理方法，針對較糟情況的資料樣式做資料的反轉減少基板效應的影響進而改善讀取電流。使用以上三種電路架構，不僅消除讀1之雜訊效應並大大增加讀0之感測邊界以及讀取電流，如此便可降低操作電壓且加快讀取速度。

我們完成兩個低操作電壓、低功耗、高速度且具有百分之百編碼覆蓋範圍之256千位元反及閘型唯讀記憶體設計。此兩個反及閘型唯讀記憶體，可達到0.3伏特以下操作電壓並且在0.5伏特操作時具有超過50百萬赫茲的操作頻率。

指導教授

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- 畢業於成功大學電機工程學系，於美國賓州州立大學(Pennsylvania State University)電機工程學系取得碩士學位，後於交通大學電子工程研究所取得博士學位，2006年進入清華大學電機工程學系任教至今。
- 具備10年以上的產業界服務經驗，曾在美國New Jersey 服務於Mentor Graphic之IC-Technology Center，回國後加入台積電，後來於積丞科技擔任處長，專注從事矽智產研發以及管理的工作。
- 研究領域：記憶體電路設計，致力於高良率、低功耗、低操作電壓、3D結構之記憶體電路研究。

Abstract

Motivation

Low power applications are more and more popular in recent years, such as sensor networks, biomedical devices, aerospace technology and portable electronic products. Ultra-low-voltage operation is one of the effective ways to extend the lifetime of batteries. Many embedded systems need large-capacity read only memories (ROM) for storing fixed programs and data with complex algorithms. ROM has the advantages of small size, high reliability, low cost and low power consumption. Read only memory is a critical functional block in common system chips. NOR-ROMs provide low VDD and high speed for small-capacity applications with a short bit-line (BL); a NAND-ROM is superior for standby-dominate low-voltage applications because of lower standby current. NAND-ROM is a better choice for large-capacity and low-power applications.

Introduction

As CMOS process scaling down, the space between metal lines are compressed and induce critical coupling effect. In conventional NAND-ROM, the coupling noise, charge sharing effect and bit-line leakage current will lead to read-1 failure. A common approach to prevent this failure is to reduce the reference voltage (V_{REF}), however, due to wide cell current distribution caused by process variation, a larger read-0 margin is required. Thus, read-0 failure gets more serious. The proposed Dynamic Split Source-Lines (DSSL) scheme is implemented to split the even source-lines and the odd source-lines. While reading, the unselected source-lines are held at VDD for forming the barrier of neighboring bit-lines, which prevent the selected bit-lines from coupling noise interference and eliminate the leakage current of the other unselected bit-lines in the meantime, such that read-1 failure can be canceled. Moreover, the proposed Data-Aware Sensing Reference (DASR) scheme provides feedback to V_{REF} to enlarge read-0 margin. As data-0 is detected, V_{REF} will be raised through the feedback path and enlarge read-0 margin. To further achieve lower VDDmin, we propose a Code-Processing (CP) scheme, The CP scheme reverses the worse-case code-pattern to reduce the body effect and improve the read current. By combining the three schemes, the elimination of read-1 noise and the enlargement of read-0 margin and read current can be done, so as to reduce VDDmin and accelerate operation speed.

Expected Results

We develop two 256Kb NAND-type ROM macros, "DSSL+DASR" and "DSSL+DASR+CP", to achieve low-VDD, low-power, high-speed and 100% code-pattern coverage. The minimum VDD of these two macros is lower than 0.3V and the operating frequency is higher than 50MHz at 0.5V.