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作品名稱

適用於進階LCD顯示系統中降低記憶體頻寬及容量之嵌入式壓縮編解碼晶片設計
An Embedded Compression Codec for Memory-Efficient Applications on Advanced-HD Specification

隊伍中文名稱

啪嗒砰 PATAPON

隊長

李宇軒 中央大學電機工程研究所電子組

隊員

陳奕成 中央大學電機工程研究所電子組

作品摘要

本作品特別開發一個high-speed embedded compression (EC)演算法核心，在操作模式上，有Quality-oriented mode及Memory-efficient mode，前者採用Lossless/Near Lossless的方式來編碼，其主要以visual quality為首要考量，而後者，是要節省一定比例的記體容量、頻寬及記憶體存取功率，而節省的比例是由使用者定義。同時，為了能夠讓硬體效能達到Advanced-HD的規格，如Quad Full-HD(QFHD, 3840x2160)本作品是以Algorithm/Architecture Co-Exploration的方式來進行開發。本作品所開發之high-speed embedded compression algorithm，主要包含下列技術：(1). associated geometric probability model (AGPM). (2). content-adaptive Golomb-Rice code. (3). geometric-based binary code. (4). rate control mechanism. 以上四項技術主要是考慮到硬體架構設計效能並且兼顧編碼效率，因此在架構設計上，本作品能夠完全的應用pipelining data scheduling及parallel processing技巧來提提升硬體執行效率，因為資料相依性的問題已在演算法設計上解決，由實驗結果可以顯示，本作品編碼效率勝過以快速編碼著稱的FELICS演算法，且僅和編碼效率較好，但演算法複雜度較高的JPEG-LS僅有平均6.17%的差異，除此之外，本作品的運算資源消耗上，只需FELICS及JPEG-LS的44%和40%。

在硬體效能方面，本作品是經由CIC T18-99A梯次進行下線，並進行量測，以TSMC 0.18-um 1P6M製程和Artisan cell library所建構而成，以雙倍平下的架構下，core size為1.80x1.80 mm^2，die size為2.33x2.30 mm^2，其中logic gate count占45.30K. 其編碼能力可以涵蓋QFHD (3840x2160) @ 30fps，解碼能力可以到達QHD (2560x1440)@30fps，編碼及解碼所消耗的功率分別是23.22mW@125MHz 及22.32mW@83MHz。

指導教授

蔡宗漢　中央大學電機工程研究所電子組

- Tsung-Han Tsai received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1990, 1994, and 1998 respectively. Currently, he is a Professor in the department of electrical engineering at National Central University.
- Dr. Tsai has been awarded more than 15 patents and 150 refereed papers published in international journals and conferences. He is also a member of IEEE and Audio Engineering Society (AES).
- His research interests include VLSI signal processing, video/audio coding algorithms, DSP architecture design, wireless communication and System-On-Chip design.

Abstract

The embedded compression (EC) technique is applied to reduce the memory bandwidth and capacity in display system. In this paper, the high-speed EC algorithm is proposed for advanced-HD specification. It mainly comprises four features: (1) Associated geometric-based probability model (AGPM) is developed to construct context-modeling mechanism without context-table. (2) Develop content-adaptive Golomb-Rice code and (3) Geometric-based binary code as the entropy coding with minor order of context. (4) Provide the rate control mechanism to guarantee the saving ratio of memory bandwidth and capacity. Furthermore, it also supports two kinds of operations mode: Quality-oriented mode and Memory-efficient mode. The former term is adopted for the users who care the visual quality. The latter term can save memory capacity, bandwidth and access power. The computation-efficiency of the proposed EC algorithm is about 44% and 40% of FELICS and JPEG-LS, respectively.

The entire codec chip is implemented in TSMC 0.18-um 1P6M CMOS technology by Chip Implementation Center (CIC). The measurement result reveals that with two-level parallelism, the performance can achieve QFHD(3840X2160)@30fps for encoding and QHD(2560x1440)@30fps for decoding, respectively. The power consumption is 23.22mW@125MHz for encoder and 22.32mW@83MHz for decoder