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作品名稱

應用於38GHz區域多點分佈服務、57GHz無線區域網路和76GHz自動雷達系統之毫米波多頻帶鎖相迴路
A Millimeter-wave Multi-Band Phase-locked Loop for 38GHz, 57GHz and 76GHz Applications

隊伍名稱
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作品摘要

創作動機

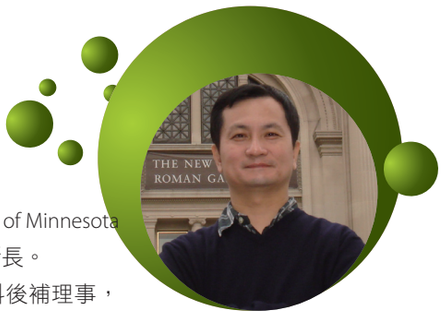
在近十年來無線通訊蓬勃的發展，藉由毫米波傳送的無線電鏈結CMOS晶片技術已逐漸成熟，也讓工業界開始重視這項技術，其應用層面包括38GHz的區域多點分布服務、57GHz的60GHz無線區域網路和76GHz的自動雷達系統等相關應用。而毫米波鎖相迴路電路在無線電系統中扮演信號源的重要角色，然而在大多數的文獻中還是著重於單頻系統的應用與探討，像是40GHz；60GHz；75GHz等這幾個單一頻帶，但多頻帶的毫米波鎖相迴路仍極少被討論到。為了因應未來多頻帶應用的趨勢，因此本設計提出一可適用於40、60和80GHz幾個頻帶範圍應用之多頻帶的鎖相迴路系統。

系統簡介

本設計之多頻帶鎖相迴路系統主要核心為一注入鎖定除頻器，其自振頻率在20GHz以達到40GHz、60GHz和80GHz的壓控振盪器之超諧波鎖定。系統之頻率範圍規劃必須從20GHz到80GHz，是相當寬頻的設計也是一大挑戰，任何電容或電感值的不匹配將會造成頻率的偏移，因此需要仔細考量並掌控寄生效應，以確保壓控振盪器的頻率範圍經除頻後可精確地落入注入鎖定除頻器的自振頻率內，此現象也嚴重地影響除頻器的靈敏度。系統之振盪信號來自三個不同頻帶的壓控振盪器電路，並利用不同的饋入技巧將信號給進注入鎖定除頻器。為了選取不同來源之壓控振盪器的信號，需內建一電流模式多工器(multiplexer, MUX)，以達到各頻帶均能精確鎖定的效果。整個迴路上包含下列元件方塊：除頻鏈共除256的除數，將振盪頻率降至參考頻率；相位頻率偵測器(phase-frequency detector, PFD)，比較振盪頻率與參考頻率的相位；電荷汞浦(charge pump, CP)可對迴路濾波器做充放電，以及一個二階的迴路濾波器(loop filter, LF)將壓控振盪器的控制電壓穩定在一直流值。

預期成果

設計出一具有多模注入鎖定除頻器(multimode injection-locked frequency divider, M-ILFD)之鎖相迴路系統，可單獨操作於40、60及80GHz多個頻段，除頻器可提供3個除頻操作模式，包括除2、除3、和除4等模式。在實際應用上可運用於汽車防撞雷達和無線高速資料傳輸等未來新潮流，並以90nm CMOS製程實現之。每個頻帶的輸出功率 > -9.5dBm，相位雜訊 < -103dBc/Hz在10MHz的偏移頻率，在1.5V的操作電壓下整個鎖相迴路消耗功率 < 114mW，使用晶片面積1.12mm^{2}於多頻帶的應用上。



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Abstract

Motivation

As the technology of wireless communication evolved in the past decades, radio links through millimeter-wavelength (mm-wave) in CMOS technology has become reality. Consecutive breakthroughs lead to an increasing attention for the industrial purposes, which include 38 GHz for Local Multipoint Distribution Service, 57 GHz for 60 GHz WLAN, and 76 GHz for Auto Radar System. As a signal source supplier in a radio system, the mm-Wave PLL has been intensely studied, exhibiting remarkable leaps in the technical domain. However, most documents are focused on the single-band applications such as 40 GHz , 60 GHz and 75 GHz. mm-Wave PLLs with multiband functionalities are seldom discussed. It is foreseen a trend of multi-band radio in the future, therefore in this paper, a triple-band mm-Wave PLL (T-PLL) is proposed in standard 90 nm CMOS process. The proposed T-PLL is capable to provide the required signal sources for 40, 60, and 80 GHz applications by the integration of different injection modes with different divide modulus (i.e. by-2, -3 and -4) into a single frequency divider.

System Architecture

An ILFD self-oscillating at 20 GHz performs superharmonic frequency locking to the signals from 40 GHz, 60 GHz and 80 GHz VCOs. The frequency plan ranges from 20 GHz to 80 GHz, showing an extremely wide-band characteristic such that any imperfection among the capacitance or inductance predictions will result in the frequency misalignment and cause function failure. Therefore, the parasitics control needs to be carefully examined to assure that VCO's frequency ranges, after being divided, can be perfectly aligned to the ILFD's self-oscillation frequency (i.e. 20 GHz). This alignment in the frequency domain is also strongly relative to the sensitivity of ILFD because the more precise the frequency alignment is, the more easily locked the injected signal will be. We demonstrate how this frequency template can be realized accurately even without the need of a complex calibration mechanism.

Three VCOs are designed at 40 GHz, 60 GHz, and 80 GHz respectively with their outputs connected to a multi-mode ILFD (M-ILFD). During its operation, one of the VCOs will be activated by an embedded multiplexer (MUX), which is realized by controlling the biasing current of each VCO through externally input control voltages. The band selection can therefore be completed. After the selection of VCO, a M-ILFD with self-oscillation frequency at 20 GHz will start frequency dividing with corresponding modulus (divide-by-2 for 40 GHz, by-3 for 60 GHz and by-4 for 80 GHz. The PLL is completed by a cascade of a 20 GHz ring-oscillator-based ILFD (Ring-ILFD), a current-mode logic (CML) frequency dividers chain with a total modulus of 128, a phase-frequency detector (PFD), a charge pump (CP) and a 2nd -order loop filter (LF).

Expected Results:

A phase-locked loop featuring triple-band (40/60/80GHz) capability is presented in 90-nm CMOS process with a multimode injection-locked frequency divider (M-ILFD). Oscillation signals from three VCOs of different bands are injected to the M-ILFD through different injection techniques. Based on the VCO selection executed by an embedded current mode logic multiplexer (MUX), the proposed T-PLL functions at each desired frequency accurately. The close-loop is completed by following components of a divider chain with totally 256 divide-modulus, a phase-frequency detector (PFD), a charge-pump (CP), and a 2nd loop filter (LF). The output power of each band exhibits >-9.5 dBm with phase noise performance of <-103 dBc/Hz at 10 MHz offset frequency. At 1.5 V the whole PLL dissipates <114 mW within a compact size of 1.12 mm^2 for the triple-band application.