D10-100

作品名稱

適用於下世代通訊/儲存系統之超越10 Gbps的LDPC解碼器設計

Over 10 Gbps LDPC Decoder Design for Next Generation Communication/Storage Systems

隊伍名稱

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作品摘要

低密度奇偶校驗碼(Low-Density Parity-Check Codes簡稱LDPC codes)由Gallager在1960年代所發表，具有非常好的編碼增益，目前已被廣泛應用於許多數位通訊標準裡，如: 第二代衛星數位廣播(Digital Video Broadcasting - Satellite - Second Generation，簡稱DVB-S2)、全球互通微波存取(Worldwide Interoperability for Microwave Access，簡稱WiMAX)、IEEE 802.11n。LDPC codes因具有優於RS codes的錯誤更正能力，且具有比渦輪碼(turbo code)更適合實現硬體平行的架構，被視為最適用下世代高速傳輸通訊系統的錯誤更正碼。現今有線或無線傳輸系統和儲存系統對於資料傳輸速率的需求愈來愈高，在有線傳輸規格中的光纖傳輸(IEEE 802.3ae)和雙絞銅線傳輸(IEEE 802.3an)，對資料傳輸率的需求都高達10 Gbps，無線傳輸系統也由數百Mbps，發展到超越5 Gbps (IEEE 802.15.3c)的傳輸速率需求。

據此，本競賽作品即為設計傳輸速率超越10 Gbps的LDPC解碼器。此解碼器同時具有高吞吐量以及優異的解碼效能，奇偶校驗矩陣使用CP-PEG編碼方法產生，編碼率高達0.9375且具有優於PEG編碼方式的解碼效能，並針對高檢查節點維度所造成的硬體複雜度提出下列改善方法：在硬體架構的設計上採用variable-node-centric排程演算法，降低疊代次數及提升解碼速率；使用single pipelined的硬體架構來減少所需的資料儲存量；針對檢查節點和排序器的架構做改善，大幅簡化控制電路及減少暫存器使用量。此電路硬體設計比傳統實現方法節省73%的記憶體使用量，並提高解碼的收斂速度。使用UMC 90nm 1P9M CMOS製程下線實現硬體，本作品提出(2048, 1920) CP-PEG LDPC解碼器晶片面積為3.84 mm^2，能源效率為0.033 nJ/bit，在120MHz的時脈運作下能夠達到11.5Gbps的傳輸速率。

此解碼器不僅可達非常高的吞吐量，且記憶體儲存量經過最佳化，相當適合未來高速傳輸的需求，有潛力取代ITU-T所制訂的光纖通訊傳輸協定G.975，且其高編碼率的特性更可應用在固態硬碟（Solid State Disk，簡稱SSD）等儲存系統。總言之，此設計具有下列特點: (1)高傳輸速度、(2)晶片面積最佳化、(3)提升解碼效率、(4)優異的解碼能力、(5)低功率消耗。

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- 張副教授，2002年取得交通大學電子工程研究所博士學位。後進入聯發科技公司擔任副理，2003年返校擔任電子工程學系暨電子研究所助理教授，並自2007年起升任為副教授。
- 累計著有SCI期刊論文13篇、IEEE研討會論文36篇。有鑑於通道編碼在各式應用中扮演著越來越關鍵的重要角色，張教授在2006年2月與李鎮宜教授共同成立OCEAN（OverCome Error And Noise）研究群，迄今完成技術移轉共14案，分別於2007年、2008年得到國科會「傑出技術移轉貢獻獎」，2009年榮獲「經濟部大學產業經濟貢獻獎」等肯定。

Abstract

Low-density Parity-check (LDPC) codes were first introduced by Dr. Gallager in the early 1960s. Having excellent error-correcting ability, LDPC codes draw great research interests and have been adopted in many communication standards, such as Digital Video Broadcasting – Satellite – Second Generation (DVB-S2), Worldwide Interoperability for Microwave Access (WiMAX) and IEEE 802.11n. Furthermore, LDPC codes, which are more powerful than RS codes in error-correcting capability and more efficient than Turbo code in highly-parallel implementation, were regarded as the most suitable error-correcting code for the next generation high-speed communication systems. Nowadays, the data-transmission rate requirements for wired, wireless communication system and storage device become much higher. For example, the data-transmission rate requirement for wired transmission standards IEEE 802.3ae and IEEE 802.3an reaches 10Gbps, and the data-transmission rate requirement for wireless transmission standards IEEE 802.15.3c is over 5Gbps.

In order to fulfill such needs, our work proposed the LDPC decoder with data-transmission rate over 10Gbps for next generation communication and storage systems. Low-density parity-check matrix is generated by CP-PEG algorithm, which has high code-rate 0.9375 and better decoding performance than the codes generated by PEG algorithm. To solve the implementation difficulties arisen from such a high code rate LDPC, our approach has the following features: variable-node-centric sequential scheduling to reduce iteration number, single pipelined decoder architecture to lessen the message size of exchanging messages, and optimized check node unit and sorter to further compress the register number. Overall 73% exchanging message memory is saved as compared with traditional architecture. Fabricated in UMC 90nm 1P9M CMOS technology, the proposed (2048,1920) CP-PEG LDPC decoder test chip occupies 3.84 mm^2 core area and could achieve maximum 11.5Gbps throughput under 120MHz operating frequency. The energy efficiency is only 0.33nJ/bit.

This decoder not only supports ultra-high throughput but also decreases the required memory size, exhibiting great potential to replace the optical communication standard G.975. The high code-rate characteristic is also suitable for the storage devices such as Solid State Disk (SSD) application. In conclusion, the achievements of our design are high throughput, low hardware cost, enhanced decoding efficiency, excellent decoding performance and low power dissipation.