D10-014

作品名稱 **正交分頻多工系統中之低功耗全數位LINC訊號成分分解器**
A Low-Power All-Digital LINC Signal Component Separator for OFDM Systems

隊伍名稱 **天天開心隊 Happy everyday**
隊　　長 **陳燦文** 交通大學電子工程研究所
隊　　員 **蔡秉原** 交通大學電子工程研究所
指導老師 **李鎮宜** 交通大學電子工程研究所

作品摘要

LINC(LInear amplification with Nonlinear Components)技術使用高效率之非線性功率放大器達到訊號線性放大。本作品描述LINC系統中之訊號成分分解器(Signal Component Separator)，功能是把原訊號拆解成兩個固定震幅的訊號。而訊號成分分解器輸出的兩固定振福訊號即可使用高效率的非線性放大器放大，兩路經放大的訊號再相加即可得到原訊號。

本作品提出一個全數位的訊號成分分解器，並且全以標準設計單位設計，並且擁有較高的電路穩定度。此設計包含了相位計算的數位訊號處理，以及一對低複雜度的相位調變器。因為數位運算的部份非線性計算需要較大的頻寬，因此操作頻率會提高而導致功耗大幅的上升，為了達到功耗最佳化，我們將晶片切割成兩個獨立的功率區域並針對操作的條件給予不同的操作環境，在數位運算的部份，我們利用降低操作電壓的方式降低功耗，為了確保電路的穩定度，先建立低電壓下之cell library，再使用標準設計流程做硬體實現，數位運算電路操作電壓可以降至0.55V，使得功率可以減少超過50%。

此設計的相位調變利用時脈訊號通過一串延遲串，用數位控制的方式達到不同的延遲時間，因而達到不同的輸出相位，為了解決製程、電壓以及溫度對於延遲串電路的影響，此設計利用兩個延遲串完全對稱的特性，提出一個幾乎不需額外電路的預先校正的方法，經過預先校正機制，可以在各種環境變異下皆可產生256種不同的相位，並擁有ps等級的精準度，此外在此訊號成分分解器也加入了補償兩路偏差的彈性機制，可以針對兩路訊號的相位不同步做補償，以提高系統效能。

本設計使用UMC90nm標準CMOS製程完成晶片的實現，量測結果證實此晶片可在0.55V/1.0V的操作電壓之下運作，整個訊號分解器晶片的功耗小於1mW，且系統效能可符合IEEE 802.11a的規範。

Abstract

LINC (LInear amplification with Nonlinear Components) could achieve linear amplification with high efficiency. In this work we introduce the signal component separator (SCS) in LINC transmitter, which separates the phase-and-amplitude modulated signal into two constant-envelope phase-modulated signals, so they can be amplified by two nonlinear PAs. Then, the original signal can be reconstructed by combining these two signals.

In this work, a low power SCS with digital-control phase shifters (DCPSs) behaved as phase modulators is presented. The proposed design, including the phase calculation and DCPSs, is all-digital and standard-cell-based, so it can benefit from the technology size scaling and has less noise effects. To reduce DSP power consumption and maintain the DCPS accuracy, the overall design is partitioned into two independent power domains with specific supply voltages. The supply voltage of DSP blocks can be scaled to 0.55V to reduce more than 50% power consumption.

The two DCPSs are based on power-of-two delay lines. By exploiting the symmetric property of the DCPS pair, a pre-calibration scheme with small extra overhead is also proposed to keep the linearity and accuracy under different PVT conditions. In our design, the accuracy could reach ps-level. Furthermore, the phase mismatch calibration capability is also added in this design to improve the system performance.

A testing chip was implemented with UMC90nm COMS process. The measurement result has shown that this design consumes less than 1mW under the supply voltage 0.55V / 1V, and the system performance could also meet the specification of 802.11a.