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作品名稱 **十六位元每秒八千萬次取樣之類比數位轉換器取樣時脈抖動之量測與補償**
**Jitter measurement and compensation for a 16-bit 80MS/s analog-to-digital converter**

隊伍名稱 **抖什麼 Jitter What**
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## 作品摘要

時脈訊號中之抖動可藉由時間數位轉換器(TDC)量測出來並量化成數位訊號。藉由適當的校正技術可將此數位訊號對應成時脈抖動之資訊。量測出來的抖動資訊，可用在數位領域補償類比數位轉換器(ADC)因取樣錯誤造成的誤差，改善輸出之訊號雜訊比。

我們實現了一個65nm CMOS製成之7-bit、80MS/s TDC並利用此TDC量測ADC取樣時脈之抖動。我們也提出了新的TDC數位校正技術。此校正技術可在背景執行，因此不會影響ADC以及TDC之正常工作。我們提出的技術也不會受到元件或繞線不匹配的影響，也不會對取樣時脈信號的波型敏感。

本報告實現之7-bit TDC解析度為0.27ps，佔據0.1mm$^2$的晶片面積，在電源供應器為1.2V下，消耗的功率為20mW。將此TDC應用於一16-bit ADC之取樣時脈抖動量測與補償上，對於一個最佳化設計之鎖控延遲迴路，在ADC輸入為29MHz之正弦波之下，可將訊號雜訊比由71.2dB改善為77.3dB。對於一個設計不良的鎖控延遲迴路則可將訊號雜訊比由60.8dB改善為74.4dB。

## Abstract

Clock jitter can be measured and digitized by a time-to-digital converter (TDC). With appropriate calibration techniques, the output code of the TDC can be translated into the corresponding jitter information. This jitter information is then used to compensate the ADC's sampling error in the digital domain, improving its SNR performance.

A 7-bit 80-MS/s TDC was fabricated using a 65nm CMOS technology. The clock jitter of an ADC is measured by the TDC. We also demonstrate a new digital calibration technique for the TDC. The calibration can be performed in the background without interrupting the normal ADC and TDC operations. The proposed technique is immune to device and interconnection mismatches, and is not sensitive to the waveforms of the input clocks.

The resolution of the 7-bit TDC is 0.27ps. The TDC occupies a die area of 0.1mm$^2$ while consuming 20mW from a 1.2V supply. The TDC is applied to a 16-bit ADC for the clock jitter measurement and compensation. The SNR of the 16-bit ADC is improved from 71.2dB to 77.3dB for an optimized delay-locked loop (DLL) and 60.8dB to 74.4dB for an ill-conditioned DLL by the jitter correction at a sine wave input frequency of 29MHz.