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作品名稱 **一個新型全數位式高解析度可變責任週期之同步複製延遲電路**
A New All-Digital High Resolution Synchronous Mirror Delay with Variable Duty Cycle

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作品摘要

本實驗提出了一個新型全數位式高解析度可變週期之同步複製延遲電路。本電路可在三個週期內完成外部訊號(Ext_Clk)與內部訊號(Int_Clk)的同步，此外本電路還可以降低鎖定後的靜態相位誤差。本電路主要有三個創新點：第一，本電路可操作在可變責任週期(15% ~ 85%)的時脈訊號。第二，由於本電路將量測延遲迴路移到輸出驅動器之後，因此本電路可不受負載效應影響，即不管輸出負載如何改變，本電路仍可精準的控制靜態相位誤差。且當本電路操作在最高頻率時，可在一周期內完成時脈同步。最後，本電路使用的微調機制，使其可增進外部訊號與內部訊號在同步之後的解析度。當訊號同步並完成微調後，其解析度小於20 ps。此晶片以130 nm標準CMOS製程完成。本電路可操作的範圍為 300 MHz至800 MHz。當電路操作在最高頻率(800 MHz)時，且其功率消耗與均方根抖動分別為2.4 mW及0.75 ps。此電路的晶片面積為0.015 mm^2。

Abstract

This study proposes a new all-digital high resolution synchronous mirror delay (HRSMD) circuit with variable duty cycle. The HRSMD synchronizes the external clock and the internal clock in 3 clock cycles but 1 cycle locking at fastest operation frequency. Besides, the HRSMD can reduce the clock skew between the external clock and the internal clock in a chip with three innovative techniques. First, by improving mirror control circuit, the HRSMD operates correctly with variable duty cycle (15% - 85%) clock signal. Second, the HRSMD works precisely and ignores the effect of output loading changes by moving the measurement delay line beyond the output driver. Besides, it can achieve 1 cycle dynamic locking. Finally, the HRSMD can enhance the resolution between external clock and internal clock with fine tune structure. After fine locking, the maximum static phase error is less than 20 ps. The chip is fabricated in 130 nm standard CMOS process. Its operating frequency range is from 300 MHz to 800 MHz. The power consumption and RMS jitter are 2.4 mW and 0.75 ps at 800 MHz, respectively. The active area of this chip is 0.015 mm^2.