A10-133

作品名稱 **用於高速匯流排中消除串擾的平行位元填充演算法**
A Parallel Bit-Stuffing Algorithm for Crosstalk Avoidance in High-Speed Buses

隊伍名稱 **寂靜編碼 Silence**
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作品摘要

隨著網路的發展和雲端運算的技術崛起，因此有高速網路的需求，舉例來說目前IEEE正在研訂100Gbps乙太網路規格。而在高速網路交換大量的資料需要高速交換機，高密度高速交換晶片是高速交換機的核心，因此高速交換晶片在目前和未來網路應用上是不可或缺的關鍵零組件。

隨著製程技術的進步與電路操作時脈的提昇，導線間的耦合電感及耦合電容增加，進而帶來更加嚴重的串擾效應。低電壓的發展趨勢，卻又降低了系統的雜訊容忍度。

文獻上發現，只要避免任何兩條相鄰的導線上出現相反方向的信號轉變(01→10及10→01)，便能有效的降低串擾。基於編碼方式而廣被採用的技術有以下兩種：第一種為地遮蔽，此方式雖然簡單，但編碼率僅有50%；第二種為查表編碼，此方式的編碼率超過69%，但硬體實作的複雜度高。

本作品基於位元填充演算法所設計的編碼方式具有下述特性：

1.編碼率超過80%，是目前文獻上已知最佳的編碼率，也是最接近Shannon通道容量的編碼方式。
2.其複雜度與匯流排的導線數目無關，即複雜度為O(1)。
3.本演算法非常簡單且可進行平行運算，具有實用價值。
4.與製程技術無關，可以很容易地與其他消除串擾的方法結合。

Abstract

With the advances of the VLSI technologies and the increase of the clock rates in the VLSI circuits, the crosstalk effect due to coupling capacitance and inductance has become an issue in deep sub-micron designs. Furthermore, the trend toward low-voltage and low-power circuit designs that leads to higher sensitivity of the circuits to interference and noise makes the problem more challenging.

In the literature, it is suggested that one can mitigate the crosstalk effect by avoiding “opposite transitions” on any two adjacent wires. A coding scheme without opposite transitions on any two adjacent wires is called a forbidden transition code (FTC).

Ground shielding is the simplest way to generate FTCs, but the coding rate (throughput) is only 50%. In 2001, Victor and Keutzer showed that there exist FTCs that achieve the coding rate 0.6942 when the number of wires is sufficiently large. However, the hardware complexity is too high to be implemented.

In this work, we propose a parallel bit-stuffing algorithm to generate FTCs. The encoding scheme features as follows:

1. Our parallel bit-stuffing encoding scheme achieves a coding rate more than 80% and very close to the Shannon capacity. To the best of our knowledge, it has the highest coding rate (throughput) among all practical encoding schemes known in the literature.
2. The time complexity of the parallel bit-stuffing encoding scheme is O(1), which is independent of the number of wires in the buses.
3. Our parallel bit-stuffing encoding scheme is very simple to implement. Therefore, our work is very practical.
4. The bus encoding methodology is independent of VLSI technology, and thus could be integrated with other techniques for crosstalk elimination in high-speed buses.