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作品名稱 **適用於下世代手機通訊之 LDPC Convolutional Code編解碼器設計**
LDPC Convolution Codec Design for Next Generation Mobile Communications

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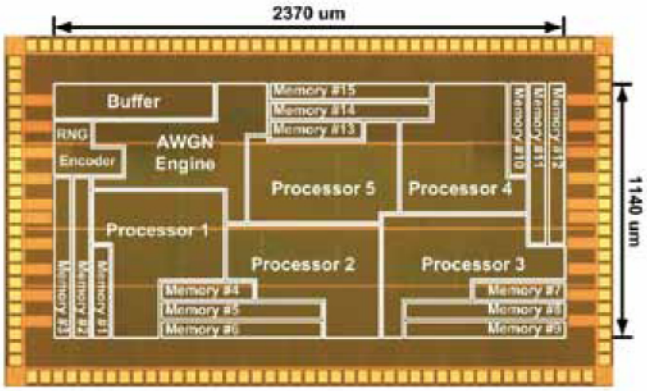
作品摘要

行動通訊系統中，通道編解碼模組往往扮演關鍵角色，不僅要達到高吞吐量的傳輸需求，也必須降低伴隨而來的功率消耗，以提供具有技術競爭力的解決方案。低密度奇偶校驗迴旋碼（LDPC convolutional codes，簡稱LDPC-CCs）於1999年提出，此碼具有彈性的碼率與區塊長度、簡單的編碼電路、較低的繞線複雜度，相較於渦輪碼（Turbo codes），更易於實現高速的吞吐量並且降低功率消耗。

據此，本作品提出演算法、節點、位元等三個層級的最佳化架構來提升吞吐量、減少硬體花費及降低解碼延遲時間，並藉由混合分割式FIFO架構來降低功率消耗。演算法層級最佳化可加速解碼收斂速度，減少一半所需的處理單元，節點層級最佳化可將平行度提高到12，並同時降低解碼延遲12倍。使用UMC 90 nm製程下線，在1.2V電壓下晶片實際量測到198 MHz，資料吞吐量高達2.37 Gbps，解碼器部分晶片面積僅佔2.24 mm2，功率消耗為284mW，能源效率為0.024 nJ/bit/proc。總言之，此作品在各方面都具有極高的競爭力，相當適合於未來使用手持行動裝置的高網路傳輸速度要求。



實作晶片圖
(包含完整的低密度奇偶校驗迴旋碼解碼器以及測試電路)

ABSTRACT

In mobile communication system, channel coding modules used to play an important role. To provide a highly competitive solution, reaching high data-transmission rate is required, so does reducing the high power consumption. Low-Density Parity-Check Convolutional Codes (LDPC-CCs) were introduced in 1999, which possess flexible code-rates, variable length of data frame, simple encoding circuitry, and low routing complexity. Compared to the Turbo decoder, the LDPC-CC decoder is more suitable for highly-parallel implementation and low-power architecture.

Therefore, our work proposed three level optimization techniques, including algorithm-level, node-level and bit-level, to increase decoding throughput, lessen hardware costs, and reduce decoding latency. Moreover, a hybrid-partitioned FIFO structure is presented to further reduce power consumption. The algorithm-level optimization accelerates the decoding convergence, which leads to the result that only half number of processors is required under the same BER performance. The node-level optimization can increase the parallelism to 12, and reduce 12 times of the decoding latency concurrently. Fabricated in UMC 90nm 1P9M CMOS process, the proposed LDPC-CC decoder chip could achieve maximum 2.37Gbps under 198 MHz operating frequency. The decoder containing 5 processors only occupies an area of 2.24 mm2 and draws 284mW with an energy efficiency of 0.024 nJ/bit/proc. In conclusions, our proposed LDPC-CC decoder outperforms state-of-the-art designs and is suitable for the high-speed transmission requirements of next-generation handheld mobile devices.