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作品名稱 **一個三維晶片高速效能自我測試使用之雙緣夾擊技術**
A High-Performance Self Test Using Double Edge Clipping Technique for 3D Chip

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作品摘要

目前的電路延遲測試是使用測試機台(Automation Test Equipment；ATE)來測試，但由於電路的低電壓設計及雜訊電壓等所引起的待測電路發生延遲，都造成使用ATE或掃描測試技術均難以正確擷取電路輸出端的延遲時序，因此本論文提出一內嵌式電路延遲自我測試Delay BIST之方法。我們所設計Delay BIST電路可以達到的效果有(1)輔助待測電路(CUT)能夠被高速進行電路延遲測試(2)經由雙緣夾擊可以量測到CUT的最高工作頻率(3)數位控制脈衝波產生器(Digital Controlled Pulse Generator ；DCPG)的粗調跟細調控制信號提供高解析度量測。本設計使用TSMC 0.18 um 1P6M的製程完成晶片下線，並且結合低速測試機台驗證我們所提的方法可使用於測試高速電路，現行低速機台將可以藉由這種設計來銜接延伸裝置來測試高速電路，讓現行的低速測試機台可繼續沿用。

ABSTRACT

The testing of system design integrated circuit is highly complex. There are many test challenges generated from at-speed delay testing requirements. BIST circuit can help to solve traditionally slower ATE tester problems. In this research, a double edge clipping technique is proposed for at-speed BIST testing. It differs from traditional circuit delay testing techniques by changing the clock rate using external ATE. This method uses lower-speed input clock frequency, then applies internal BIST circuit to adjust clock edges for circuit high-speed delay testing. Test chips are fully validated. The post-layout simulations show that the wide-range (36%~74%), fine-scale (14.3ps), coarse-sacle(334ps) duty cycle adjustment technique with high-precision calibration circuit is effective for at-speed delay testing and performance binning.