Design Group D11-094

作品名稱

採用脈衝縮減器並具寬範圍數位自我校正之高精度數位脈衝寬度調變器

A Wide Range And High Accuracy Digital Pulse Width Modulator with Digital Self-Calibration Based on Pulse Shrinker

隊伍名稱
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作品摘要

在高度科技化的現代社會裡，許多的電子產品都往體積小、功能大的方向發展，就以最常見到的電源管理IC領域而言，應用層面極廣，在相關市場上一直以來都扮演相當重要的角色，且在許多3C產品都需要使用電源管理IC，並且強調其特性需要高精準度、小面積、低功耗，以符合當前節能省碳的重要環保課題，並講求設計功效最佳、品質最穩的元件，以供應市場發展需求。近年來又以數位脈衝寬度調變（DPWM）方法為發展主題，許多人紛紛投入此研究領域，開創DPWM之嶄新應用。

除此領域，DPWM目前運用的範疇很多，我們常見到的另一項使用範例是以PWM技術來控制馬達轉速，近來在LED驅動電路上也都採用DPWM來做為調光電路，透過不同的脈衝寬度決定LED之通電發光時間週期，不同比例導通週期進而決定LED之亮暗程度差別，未來更甚至可以運用在LED混光調整。另外，我們也看到，漸有文獻提出以PWM概念實現Class-D放大器等電路，顧我們更期待未來數位脈衝寬度調變電路之應用愈來愈廣泛，進而在證明本電路之優越價值性。

我們參閱目前LED驅動電路架構以及電流轉換器架構文獻，分析其優缺點，提出電路設計，僅需要簡單的創意概念，立即可以達到極佳的效能。本晶片設計希望透過此次機會將先前創意設計的DPWM在更精近實現出來，構思更為簡單的電路架構，並以類比IC形式去實現電路，希望如此可以提高電路之精準度，並設法減少電晶體的使用數量，節省電路面積，提高其操作之速度，有效提升DPWM電路之效能。

本次我們在創新架構上力求創新，簡單利用反相器概念節省一半的延遲線，所以在解析度高達12bits時面積可以有優越表現，並且降低功耗，又有數位校準功能，達到97kHz～2MHz超寬範圍切換頻率的應用，可想而知其未來的應用值得期待，無論應用於LED調光、電源管理IC、Class-D放大器…各項電路，都可以有很好的表現。我們突破傳統的迷思，提升電路效能並不需要複雜化電路，反而應該用創新的概念、用效果好有創意的簡單電路，就達到功能效果極佳的電路設計，如本次參賽的DPWM，就是一項成功的設計。

圖一 本創意設計DPWM應用領域廣泛

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- Poki Chen was born in Chia-Yi, Taiwan, R.O.C., in 1963. He received the B.S., M.S. and Ph.D. degrees in Electrical Engineering Department from National Taiwan University (NTU), Taipei, Taiwan, in 1985, 1987 and 2001, respectively.
- During 1998-2001, 2001-2006 and 2006-2011 he was a Lecturer, an Assistant Professor and an Associate Professor correspondingly in Electronic Engineering Department of National Taiwan University of Science and Technology (NTUST). He is a Professor in the same department now. Since 2010, he was selected as the director of System-on-Chip Research Center, NTUST. Currently, he serves as an Associate Editor for IEEE Transactions on Very Large Scale Integration (VLSI) Systems.
- Research focus: Analog / mixed-signal integrated circuits and systems with special interest focused on time-domain signal processing circuits, such as time-domain smart temperature sensor, timeto-digital converter (TDC), digital pulse generator, digital pulse width modulator (DPWM) and duty cycle corrector (DCC). He is also interested in creating innovative analog applications for FPGA platforms, such as FPGA smart temperature sensor, FPGA digital-to-time and time-to-digital converters.

ABSTRACT

Nowadays, the electronic devices have rapidly developed due to the market demand. The devices have been produced in larger scale production, faster speed and smaller size. Most devices use integrated circuit (IC) or chip to have small size. The product features can be commonly seen in gadgets or 3C (Computer, Cell phone and Camera). In contrary, the available power decreases. Therefore, products with low power, good quality and small chip size are demanded. The main part to overcome this issue is to have devices with a good controller with a good power management.

As result, controller recently has shifted from analog- to digital-controllers since digital controller has lower power consumption and faster speed application. The most common application is for DC-DC converter. Its performance is much depending on the resolution and performance of Digital Pulse Width Modulation (DPWM) to avoid limit-cycle oscillation. In Addition, the role of DPWM in electronic device can be widely seen in controlling the speed of motor. Recently, DPWM is also occupied in LED driver for dimming circuit such as at traffic light and LED screen for TV or computer. A variety of pulse width determines the LED power of light-emitting time periods to have different proportions of light emitting-cycle to adjust the degree of brightness. Furthermore, DPWM is employed in Class-D amplifier such as in sound system. High resolution and good performance DPWM will also affect the quality output of the sound. More widespread DPWM applications will be found in the future.

From the reasons above, high performance and high resolution 12-bit DPWM is developed. This DPWM is based on pulse shrinking delay line. By reducing delay line about a half in exchange of occupying one inverter, it has extremely simple structure. To reduce the impact of cell mismatch on delay line, a serpentine layout is adopted. The layout is made as squared as possible to minimize gradient effect. With this layout, the tapped output of the delay line can be addressed through proper row and column selections. Thus, the digital multiplexer that usually consumed much area will become smaller by using an address decoder and transmission gates to tap out the DPWM output. Fabricated in a TSMC 0.18-μm 1P6M standard CMOS process, the chip size is only 0.751 mm2. By digitally calibrating the amount of delay line pulse shrinking with successive approximation (SAR), the DPWM can achieve 97 kHz ~ 2 MHz wide range operation frequency and 1.249 mW low power consumption at 1 MHz. Moreover, the DPWM reveals excellent performance in linearity and stability. The INL measurement is -0.32 ~ +0.21 LSB at 2 MHz. With inaccuracy less than 0.5 LSB, it ensured all input bits of the DPWM are valid. Therefore, this DPWM circuit is applicable for low cost, low power, small chip size, and good performance DPWM applications as stated above as well as for many future implementations. With a Figure of Merit (FOM) similar to ADC's, the proposed circuit owns 10248.2, the best than ever figure to ensure its superiority.