Design Group D11-118

作品名稱

三維構裝晶片的多電源低功率設計技術與電壓量測機制

Multi-Voltage Low Power Design Technique with Built in Voltage Measurement Mechanism for 3D-CHIP

隊伍名稱
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作品摘要

3D IC設計中的一個主要問題便是電源供應的問題，因為如何有效的供應堆疊的晶片所需的各種電源便是一個亟待解決的問題。3D結構將產生比傳統的2D晶片有更為嚴重的電源壓降與電源干擾的問題，上述兩種問題皆會導致電路設計中的延遲時間增加，不僅會導致晶片效能下降，甚至可能出現晶片無法正常工作的狀態，嚴重影響晶片的可靠性。為了精確的評估3D IC所產生的電源問題，在本論文中，我們去設計一個可以針對3D多電源結構的低功率設計技術與電壓品質進行量測的機制。在這個設計中使用多電壓源來設計一個三維結構晶片。在這個設計中我們研發了低消耗電流之高低電壓轉換開關控制電路（PSCC），與暫存型Flip-Flop（retention FF）可把電路整個電路的動態功率消耗最少。我們設計的RetFF可以允許的power off無電源時仍可操作45個clock cycle，正確維持logic state，因此可以節省電路工作與暫眠模式狀態轉換時間及功率的消耗。晶片實際量測結果，證明運用PSCC電源控制機制可以讓整顆CHIP節省95% 尖峰電流消耗，而CKVdd模式的省電效果最高可達94%，並且我們可以透過Retention Flip-Flop的儲值功能，又可讓CHIP再節省29%功率消耗，是一個具電源管理功能的有效低功率設計。

在這個設計中我們主要是在發展三種設計技術。第一種是晶片中的低功率技術，可以提供電源具有高低電源、休眠、CKVdd等四個操作模式，配給電路效能功耗在不同模式操作。提供三維結構設計低功率的設計技術，希望結合功率管理解決三維設計功耗大的問題。第二種是電源品質量測的功率管理機制，達到維持三維結構設計的電源穩定品質。第三種是無電型暫存器的設計，供三維設計中的電路在電源品質不佳或處在休眠的模式時，可將電路的運算結果暫存，既可節省功率又可以克服電源干擾電路的問題，維持整個複雜的三維電路可正確操作。

我們將所設計的晶片採用MorPack技術作三維疊接，採用前述單一晶片的低功率設計機制，經過初步驗證的結果說明較二維晶片而言其效能的增加與功率的降低，從量測結果都可明確得到證明，Pad的功率節省達86.7 %，系統效能增進36 %。

圖一 三維晶片疊接後之結構圖

指導教授

鄭經華 逢甲大學電子工程學系

- 畢業於中正大學資訊工程所博士班，目前任職於逢甲大學電子工程學系擔任副教授。
- 鄭老師專注於高速動態電路與低功率電路之設計、測試與實作，其實驗室在高效能、低功率設計測試技術與晶片實作上都已具備相當好的基礎；並且在電路設計、流程整合、晶片實做驗證及應用系統端之整合、以及與中正大學SoC團隊在低功率多媒體視訊IP晶片實作、系統整合與驗證平台合作上，都獲得相當不錯的成果。
- 專長領域：VLSI Design/Test/CAD。

ABSTRACT

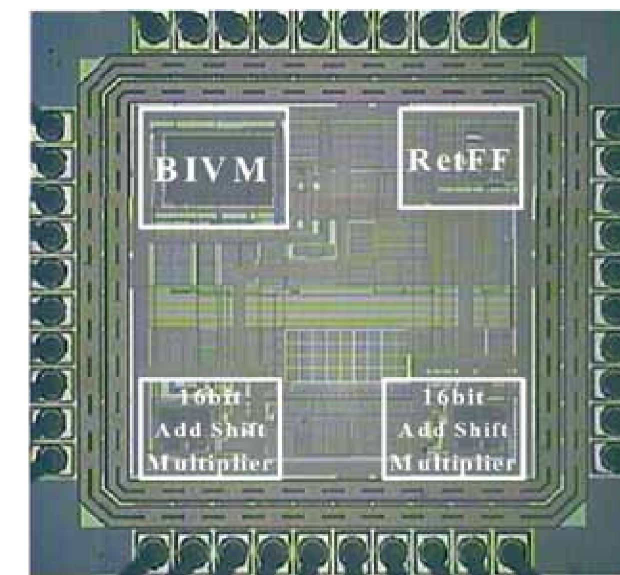
Due to the increase in integration densities required from system application demand, a chip contains devices. Moreover, continuing shrinking device sizes leads to longer wire-lengths which causes interconnect delays to critically impact chip performance. Three-dimensional integrated circuit (3D-IC) is one promising technique for resolving this problem.

In 3D-IC, the multiple supply voltage (Vdd), ground (Vss) and body bias (Vth) turning techniques are applied to the core and IO interface circuits. This will lead to complicated power source track distribution design within the package. 3D-IC power integrity research topics can be divided into several categories. In design issues for 3D-IC -- especially for multi voltage domain design within each layer --includes: 1.How to make suitable circuit partition based on power consumption and to equalize the power distribution of each layer for minimizing the heat. 2. Voltage-drop measurement IP circuit design and implementation. 3. Power track physical design techniques. 4. Power supply plan--partition/distribution techniques. 5. Efficient multiple layer power connection techniques. 6. Different power distribution techniques for different stacking styles.

Multiple voltage (multi-Vdd) technique is an effective low power design technique to reduce power consumption. For multi-Vdd designs, most chip failures are due to power supply problems of voltage drop and noisy voltage. Several low power design techniques are proposed in this report, such as power switch control circuit, retention Flip-Flop. A Built-In Voltage Meter (BIVM) is proposed for chip internal voltage level observation. This measurement mechanism can accurately identify the voltage level variances for debugging chip popular failures such as performance degradations.

A feasible low-cost 3D stacking design method is proposed. Multiple voltage design technique is applied to reduce power consumption. A low-power built-in digitalized power-aware management mechanism for multiple voltage domain design is adopted. A power switch control circuit is used to support multiple operation modes for multiple voltage designs. A BIVM is used for internal voltage level observation. A powerless retention flip flop is applied for temporary data storage. These efficient power-aware adjusting mechanisms are successfully validated by a low-power, noisy-voltage tolerant 64bit multiplier using a low-cost 3D stacking technique.

These topics are physically implemented and silicon proven using advanced TSMC process from Chip Implementation Center. The 3D stacking design includes multi-Vdd low power design technique and BIVM are successfully evaluated.



圖二 單一晶片之照相圖