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**A Low-Power 300-MS/s 10-Bit Pipelined ADC with Automatic Biasing**

一個自動偏壓的 **300-MS/s 10-Bit** 低功率管線式類比數位轉換器

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## 作品摘要

管線式類比數位轉換器是目前被廣泛使用在許多寬頻無線或有線的通訊系統應用上，可以達到高速、中高解析度等多數應用上的要求。但轉換器需要搭配高精準度的類比電路，才能得以實現。但是在先進製程的演進下，元件本質增益下降、匹配度變差以及操作電壓下降，都使得高精準度的類比電路設計變得相當的困難。同時，先進製程元件參數的變異度大，並且會隨著擺放位置和周圍電路的不同而變化。這使得一些需要良好元件匹配度才能正常工作的電路，例如：電流鏡，在設計上面臨更大的挑戰。此外，由於製程、操作電壓以及溫度（PVT）的變動，所造成元件參數和匹配度的變化，都會導致轉換器的效能下降。因此，為了避免PVT變動所造成的影響，在電路設計上就必須要保留更大的設計邊際和更多的模擬次數，來涵蓋因為PVT變動所造成的影響。產生更多的額外功率消耗和設計模擬時間。

本作品設計出了一個強韌、高速、高性能和低功率消耗的類比數位轉換器，可以克服先進製程以及PVT變動的影響，並且可以隨著先進製程一同做演進。包含了三個主要部分：

（一）設計一個高速的切換放大器。可以節省約50%的放大器功率消耗，並同時合併了下一級的輸入取樣開關，提昇操作速度。

（二）使用背景式的數位校正技術，來改善因為類比電路精準度不足和PVT變動所造成轉換器效能下降的問題。所有的校正動作都是在背景下完成，不會影響轉換器正常的操作。

（三）使用自動偏壓技術來產生電路所需要的偏壓。整個轉換器沒有使用到任何外部偏壓源和電流鏡形式的電路。所以不需要匹配度良好的元件，可以克服先進製程元件參數變動過大以及PVT變動的問題。可以大幅的降低設計時所保留的邊際，降低額外的功率消耗和模擬時間。同時提昇產品在量產時不同批晶片之間的良率，並且讓轉換器在不同的操作頻率下，都能有較低功率的消耗。

本作品將上述所提出的技術全部整合到一顆晶片，設計了一個10-Bit 300MS/s的管線式類比數位轉換器來驗證所提出的技術。使用65奈米的CMOS製程來實現，操作電壓為1.0伏特。根據實際晶片的量測結果，輸入訊號的有效頻寬（ERBW）可以達到304MHz。作品中所提出來的高速切換放大器，是目前已知文獻中使用此技術而可以達到的最快操作速度。而背景式的數位校正技術也被驗證可以有效並大幅的改善轉換器的精確度。而自動偏壓技術，在不同的溫度和操作電壓的變化下，也被驗證可以使得轉換器的輸出效能，都能保持固定並有較小的功率消耗。

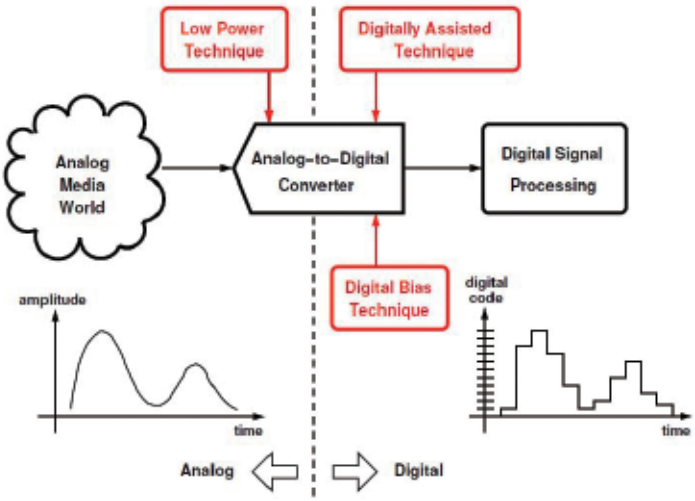


圖1 > 一個強韌、高效能和低功耗的通用型類比數位轉換器設計
A robust, high-performance and low-power general-purpose analog-to-digital converter design

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**研究領域**

Mixed-signal integrated circuits. Data conversion techniques. Ultra low-power integrated circuits.

## Abstract

Pipelined ADCs are now widely used in broadband wireless or wired communication system applications, to achieve high-speed, medium-to-high resolution for requirements of most applications. But the converters need with high-precision analog circuits to achieve good performance. But in the evolution of deep submicron process, the nature of the lower intrinsic gain, matching deteriorated and lower supply voltage that have made high-precision analog circuits design becomes quite difficult. Meanwhile, the parameters of deep submicron devices are with large variations, and varying with their position and surrounding circuits. This makes the some circuits that require good matching circuit to work properly, for example: current mirror, the design face greater challenges. In addition, due to process, the supply voltage and temperature (PVT) variations caused the component parameters and matching property changed, will lead to decreased performance of the converter. Therefore, in order to avoid the impact of PVT variations, the circuits design must be designed to retain a greater design margin and more simulations to cover because of the impact of PVT variations. It requires more additional power consumption and design simulation time.

This work designed a robust, high-speed, high performance and low power consumption analog-to-digital converter, can overcome the impact of deep submicron process and PVT variations, and can follow the evolution of advanced process to scale down. It is consisted of three main parts:

(1). A high-speed switching opamp is designed to save about 50% of the power consumption of the opamp and merged with the input sampling switches of the next stage, increase overall operating speed.

(2). Digital background calibration is used to correct the A/D conversion errors caused by the low dc gain of the opamps and devices mismatch. It can improve the accuracy of the ADC effectively, and insensitive to these non-ideal characteristics. The operation of the digital calibration is performed under background, so it will not interrupt the normal operation of the ADC and not influence the analog signal path. Performance degradation causing by PVT variations, the digital calibration techniques can effectively correct back and improve the accuracy of the ADC.

(3). Automatic bias technique is used to generate the required bias current. The acquired calibration data are used to monitor the settling behavior of the opamps. The bias currents in the opamps are then automatically adjusted by digital control circuits such that the settling behavior can be maintained without generating excessive current consumption. Neither external bias generator required, nor current mirror used. Since the automatic biasing technique does not require any matching accuracy requirements. It can be used to overcome the changes of the devices characteristics due to the placing of the different locations and the surrounding circuitry in the advanced nanoscale process. The automatic biasing technique is insensitive to fluctuations in fabrication process, temperature, and supply voltage. Therefore, the design margins for each bias current of the opamps can be further minimized on a chip by chip, both reduction of power dissipation and a higher yield in mass production can be achieved. Besides, the power consumption of the ADC can vary linearly with the sampling rate and maintain the minimum power consumption in various operating frequency.

To demonstrate the above techniques, a 300MS/s 10-bit pipelined ADC was designed and fabricated using a 65 nm CMOS technology. All techniques which mentioned above are integrated in the same chip. The supply voltage is 1.0 V and occupies die area of 0.36~mm^2. According to the measurement results of the chip, the effective resolution bandwidth (ERBW) of the input signal is up to 304MHz. The proposed switching opamps can save the power consumption. In the current published literatures, the proposed switching opamps can achieve the fastest operating speed. The digital background calibration can significantly improve the ADC accuracy efficiency. And the automatic biasing technique can retain the ADC performance with minimal power consumption under PVT variations.