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Active Noise Cancellation Chip Design for Single Microphone In-Ear Earphones

適用於單麥克風內耳式耳機之主動抗噪晶片設計

隊伍名稱
主動式抗噪晶片小組 / Active noise cancellation chip group

隊長
翁國原 逢甲大學電子工程研究所

隊員
Hong-Son Vu Ph. D. Program of Electrical and Communications Engineering
孫仕峰 逢甲大學產業研發碩士專班
馮天懋 逢甲大學電子工程學系

指導教授
陳冠宏 逢甲大學電子工程研究所
王　壘 逢甲大學電機工程研究所

作品摘要 Abstract

由於傳統的耳罩式主動式抗噪耳機體積太大、攜帶不方便，近期主動式抗噪耳機，往內耳式主動抗噪耳機發展。但由於內耳式耳機尺寸小，所以於感度、 頻域等音質相對較差；因此，為突破過去基於傳統經驗法則之設計框架，並結合現今最新的軟硬體優勢，我們提出一個利用晶片結合內耳式主動式抗噪耳機來達成低功耗、小面積等優勢，以增加實用性，並結合晶片的快速運算達到即時消除噪音的效果。

本作品實現一適用於單麥克風內耳式耳機之主動抗噪晶片設計，以雙麥克風前饋式演算法架構為基礎。經由改良演算法，可只使用單麥克風即達到主動式抗噪效果，節省硬體成本與體積。硬體架構創性部分，我們在適應性濾波架構中加入管線化架構，提升迭代運算速度，並設計一客製化記憶體以快速存取大量的運算資料。經由field-programmable gate array（FPGA）驗證，能有效消除325~875Hz頻帶之外部噪音。最後，我們採用標準Cell-based設計流程，並使用TSMC90GUTM製程，成功完成此適用於單麥克風內耳式耳機之主動抗噪晶片之設計、實作與驗證。

This work proposes an efficient active noise cancelling (ANC) circuit design for the in-ear headphones. We develop a hardware oriented Least Mean Square (LMS) adaptive algorithm, and design a modified high-performance feed-forward ANC architecture which only uses one microphone to effectively cancel broadband noise for the in-ear headphones. The proposed ANC circuit design has been successfully implemented through adopting the standard cell-based design flow based on the TSMC 90nm CMOS technology. Besides, the proposed design has been verified under versatile noisy scenarios for its real-time ANC performance by using a Field Programmable Gate Array (FPGA) platform. Experimental results show that the proposed high-performance circuit design can reduce disturbing noise of various frequency bands very well, and outperforms the existing works. The proposed design can attenuate the broadband pink noise between 325 Hz to 875 Hz, with a maximum performance of 18dB. Moreover, the proposed design can achieve 406.5 M samples/sec data throughput rate at operating frequency of 50 MHz, at the costs of 111.7 k gates and 3.50 mW of power consumption.

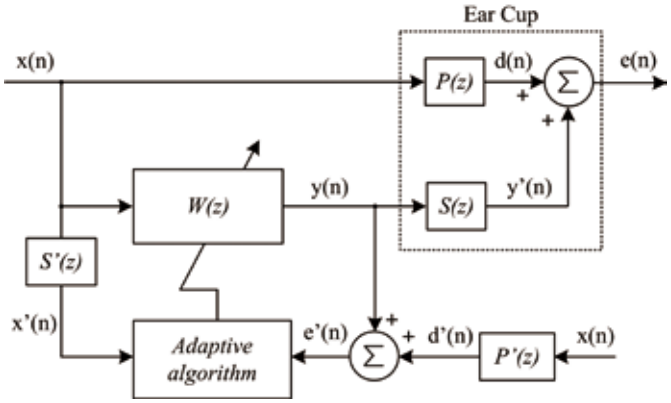

圖1 > 系統架構圖