隊伍名稱
點子王 / King of Idea

隊長
李欣儒 交通大學電子研究所

隊員
林佳龍 交通大學電子研究所
楊志文 交通大學電子研究所

指導教授
李鎮宜 交通大學電子研究所
張錫嘉 交通大學電子研究所

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Stochastic LDPC Codec Chip for Wireless Personal Area Network Applications

應用於無線個人區域網路之低密度同位元檢查碼隨機編解碼器晶片

作品摘要 Abstract

本作品提出一個應用於無線個人區域網路之低密度同位元檢查碼編解碼器，具有高吞吐量、低功耗且支援四種碼率的優點。我們使用了隨機解碼演算法來降低傳統最小和解碼器在晶片設計上之繞線複雜度與功率消耗；同時由於運算單元的簡化，解碼器的操作頻率可大幅提昇。另外，為了支援不同碼率與權重的同位元檢查碼，我們提出了可變節點的硬體架構以及繞線網路重排的技巧來提升晶片利用率。考量到晶片測試的不穩定性，本作品亦將編碼器、高斯通道產生器與解碼器整合為一完整編解碼器系統；同時我們也設計了一個具有獨立電源區域的延遲鎖相迴路來提供晶片內部高速且穩定的時脈源。根據前述特色，本作品透過聯電90奈米下線並經由CIC數位量測機台進行量測，結果顯示本作品的晶片面積為2.67 mm^2，可達到90 %的晶片利用率；在供應電壓為1.2 V下，可以達7.92 Gb/s之晶片吞吐量且僅有437.2 mW的功率消耗，相對應的硬體效益及能量效益為2.97 Gb/s/mm^2及55.2 pJ/bit。相較於現有應用於IEEE 802.15.3c的解碼器中，本作品可達到最高的硬體效益及能量效益。

This work presents the first silicon-proven stochastic LDPC decoder to support multiple code rates for IEEE 802.15.3c applications. The critical path is improved by a reconfigurable stochastic check node unit (CNU) and variable node unit (VNU); therefore, a high throughput scheme can be realized with 768 MHz clock frequency. To achieve higher hardware and energy efficiency, a reduced complexity architecture of tracking forecast memory is experimentally investigated to implement the variable node units for IEEE 802.15.3c applications. Based on the properties of parity check matrices and stochastic arithmetic, the optimized routing networks with re-permutation techniques are adopted to enhance chip utilization. Considering the measurement uncertainties, a delay-lock loop with isolated power domain and a test environment consists of an encoder, an AWGN generator and bypass circuits are also designed for inner clock and information generation. With these features, our proposed fully parallel LDPC decoder chip fabricated in 90-nm CMOS process with 760.3K gate count can achieve 7.92 Gb/s data rate and power consumption of 437.2 mW under 1.2 V supply voltage. Compared to the state-of-the-art IEEE 802.15.3c LDPC decoder chips, our proposed chip achieves over 90% reduction of routing wires, 73.8% and 11.5% enhancement of hardware and energy efficiency, respectively.