D14-105

Using Programmable Delay Measurement in Digital Voltage Adjustment for Power Management Design

使用延遲可規劃之數位式電壓調節電路的設計與實現功率管理

隊伍名稱

一尾變兩尾 / One to two

隊長

田靜樺 逢甲大學電子工程學系

隊員

方毅瑋 逢甲大學電子工程學系

作品摘要

這個電路設計目的在考量系統晶片在運算時需不斷的改變電壓且減少功率浪費，我們的設計可彈性調整外接的供應電壓達成系統晶片消耗較低功率的期望。我們設計的電路中主要分為三個部分，其中包含雙電壓源供應，與電壓比較機制，以及控制電壓源機制，我們將此雙電源設計在晶片上，依效能與功率消耗區分可為三段的調節模式：高電壓、低電壓與休眠，因為雙電源的設計，所以待測晶片上電壓供應的管理與分布會變更加的複雜。 電路設計原理是藉由判斷外接電路產生的壓差在運作時，造成比較電路運算速度上的差別，再用Flip-Flop來進行分別，藉由判斷電路以及控制電路去控制電壓，改變電壓源開關，再回饋給外接電路，如此重複判斷外接電路在運作時所造成的電壓變化並且進行調變，進而修正至不影響運算效能的穩定電壓。 此設計使用數位電路來調節電壓，除了可規劃的調整改變電壓的靈敏度，另包括自動化合成的電路設計，也可以很容易地結合其他電路做在單一顆晶片上，設計目標是動態控制晶片中各個子系統的電源電壓。未來SoC 晶片裡需要具備有這樣的功率管理單元，將可使整個系統晶片達到低功率高效能的需求。

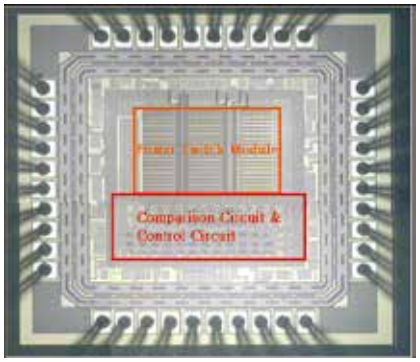

圖1 > DIE

圖2 > 本晶片與H264系統連結

2014

指導教授

鄭經華 / 逢甲大學電子工程學系

畢業於中正大學資訊工程研究所，目前任職於逢甲大學電子工程學系，專注於高速動態電路與低功率電路之設計、測試與實作。整個實驗室團隊在高效能、低功率設計測試技術與晶片實作上都已具備相當好的基礎。並且在一些原創性技術（CKVdd 與 VDP）獲得很好的成果，這些研究成果包含電路設計、流程整合、晶片實做驗證及應用系統端之整合。並與交通大學郭峻因團隊在低功率多媒體視訊 IP 晶片實作、系統整合與驗證平台建立密切合作，有相當不錯的具體成就。

研究領域

超大型積體電路設計 VLSI design、超大型積體電路測試 VLSI Testing、超大型積體電路電腦輔助設計 VLSI CAD。

Abstract

This design uses a digital circuit to regulate the voltage, in addition to adjusting the programming voltage sensitivity, and the automated synthesis circuit design can easily be combined with other circuits on a single chip. When the circuit was designed that it could continue to change the voltage and the resulting power would be reduced during the operation. In order to meet the expectations of the external circuits have low power consumption. The voltage supply management and distribution of the chip become more complex. The circuit is mainly divided into three parts in our design, which includes the dual voltage supply source, the voltage comparator, and the voltage sources control mechanism. This chip designed by dual voltage, and it is according to performance and power consumption that it can be distinguished into three adjustment modes: high voltage, low voltage and sleep. The comparator circuit generated in the external circuit by determining the differential supplied voltage during operation, causing a difference in circuit operation speed, and then comparing by Flip-Flop chain, to control the voltage source. The judgment circuit and a control circuit, and then feeding it back from the external circuitry. This repeating operation can determine the external circuit when the voltage variation caused performance to be modulated. The correction mechanism does not affect the circuit's operation to stabilize the output voltage. The goal is to control the various subsystems' voltage can be dynamically supply to the chip. By using the proposed mechanism, the whole system can achieve low power and high-performance. In the future, there is no need to have an additional power management unit in a SOC chip.

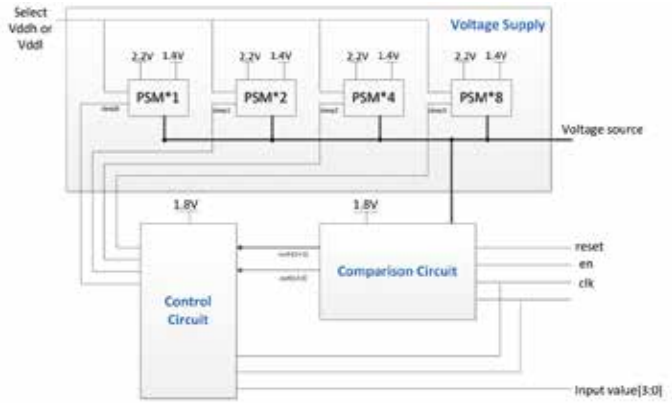

Fig.3 > The chip system structure

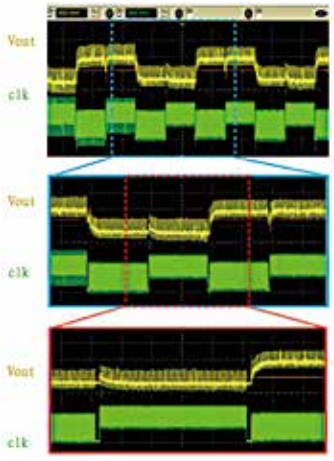

Fig.4 > The output voltage waveforms during adjustment