設計組
Design Group

D18-006

一個25-Gb/s, 2.1 pJ/bit積分型光接收機與鮑率時脈資料回復電路

A 25-Gb/s, 2.1 pJ/bit, Integrating Type Optical Receiver with a Baud-Rate Clock and Data Recovery

隊伍名稱　追光者 The Light Runner
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作品摘要

隨著網路雲端技術的進步，資料頻寬的倍數成長，為了提昇整體系統的資料頻寬，電路板與單晶片內之電性連接的通道數必須跟著提昇。然而，使用傳統銅纜線做訊號連接的方式面臨了電磁干擾、訊號高頻衰減、長度限制等諸多瓶頸；另一方面，光纖纜線應用在長距離的電信通訊（海底光纜、洲際光纜），從西元1980年代開始，已使用超過30年；在中長程距離的網路通訊（都會網路、區域網路）與數百公尺距離的資料儲存系統（資料中心、伺服器與伺服器之間的傳輸），光纖通訊也被使用分別超過了20年與10年的時間；目前在伺服器內、電路板內、晶片與晶片之間的資料連接，為了克服因銅線電性連接所造成的限制，預估將有越來越多的輸入及輸出介面將使用光連結技術，光纖將逐漸取代傳統銅線，傳輸的距離也會越來越短，可應用的產品也會更接近一般大眾。依據IDC預計，全球資料量從2013年至2020年將成長10倍，資料總量將從4.4 ZB增加至44 ZB。一個高速且節能的光接收機將可省下每一資料位元傳輸時的能源消耗，進而省下數個電廠的耗能，其結合光電、通信、及電路科技對綠色環保產生巨大貢獻。

本作品提出了一個高整合度之光接收機，包含類比前端電路、時脈資料回復電路與1對4解多工器，架構如圖一所示。光接收機採用積分型類比前端電路並整合鮑率時脈資料回復電路達到高靈敏度與高能量效益。相較於傳統需邊緣取樣之兩倍超取樣時脈資料回復電路，鮑率時脈資料回復電路將可節省約一半的佈局面積與功率損耗。除此之外，實現一個混和信號的迴路濾波器，利用類比方式累加後再使用數位方式作運算，不僅解決傳統需操作於高速之全數位迴路濾波器之缺點同時保持可程式化調控迴路頻寬機制。

在輸入資料速度為25 Gb/s、PRBS31與誤碼率小於10^{-12}的情況下並使用響應度為0.53 A/W之光感測器，量測之輸入靈敏度為–8.7 dBm，回復之資料抖動量為1.7 psrms。量測之jitter tolerance大於IEEE 802.3 ba定義之jitter tolerance mask。本作品使用台積電40-nm bulk CMOS製程實現，其核心電路面積為0.09 mm²，操作於25 Gb/s時，整個接收器的能量效率為2.1 pJ/bit。本作品在考量面積、功耗、速度、接收機敏感度等工作條件下，其整體性能指標（FoM）達到或超越現有國際一流期刊之技術水平。

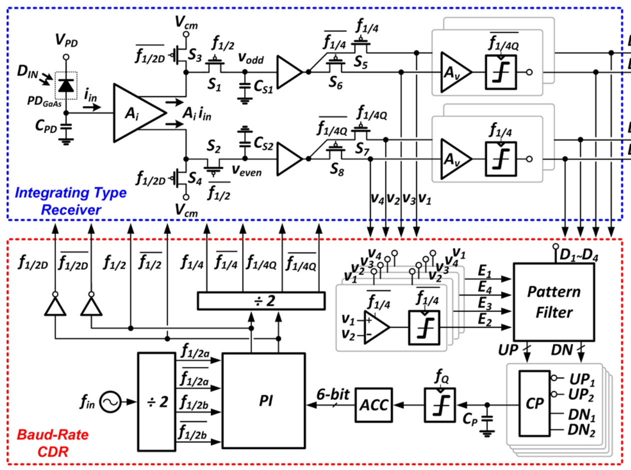

圖1. 系統架構圖

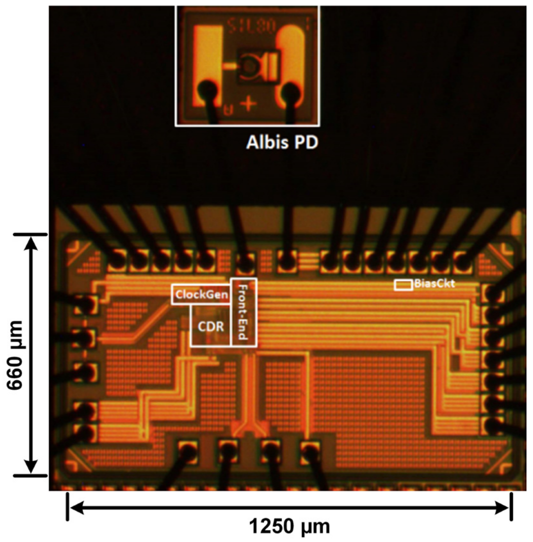

圖2. 晶片與光感測器照相圖

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研究領域

混合信號積體電路、通信積體電路、感測器電路。

Abstract

With the advancement of Internet cloud technology, data bandwidth growth is exploding. In order to increase the data bandwidth of the overall system, the number of electrical channels between the printed circuit board and the single chip must be increased. However, the use of traditional copper cables for signal connection is facing many bottlenecks such as electromagnetic interference, high frequency attenuation, and length limitation. On the other hand, the fiber optic cables used in long-distance telecommunications (submarine optical cables, intercontinental optical cables) have been used for more than 30 years since the 1980s. In the medium and long-distance network communications (both metropolitan area and regional networks) and hundreds of meters of data storage systems (transmissions between data centers, server and server), fiber-optic communications have also been used to more than 10-20 years, respectively. Currently, the data link between the server, the circuit board, and the chip to chip is to overcome the loss caused by the electrical connection of the copper cables. It is estimated that more and more input and output interfaces will use optical link technology, optical fiber will gradually replace traditional copper cables, and the transmission distance will be shorter and shorter, finally, applicable products will be closer to the general public. According to IDC, global data volume will grow 10 times from 2013 to 2020, and the total data will increase from 4.4 ZB to 44 ZB. A high-speed and energy-saving optical receiver will save energy consumption per data bit transmission, thereby saving the energy consumption of several power plants. It combines photoelectric, communications, and circuit technology to make a great contribution to green environmental protection.

This work presents the design of a highly integrated optical receiver comprising of a front-end amplifier, a CDR, and a 1:4 demultiplexer. The system architecture is shown in Fig. 1. Incorporating with an integrating type receiver front-end, a new baud-rate CDR is proposed to achieve both high sensitivity and highly energy-efficient operations. Compared to conventional 2X oversampling CDRs that require edge samples for timing adjustment, the baud rate CDR reduces the number of sampling phases by half to save area and power consumption. Besides, a hybrid loop filter consisting of analog decimation and digital post processing is proposed. It greatly relaxes the speed requirement of an all-digital loop filter while keeping the flexibility of a programmable loop bandwidth.

By applying a PRBS31 test pattern and using a PD whose responsivity is 0.53 A/W, the input sensitivities of the optical receiver at 25 Gb/s operation is about –8.7 dBm for a BER of less than 10^{-12}. The recovered data jitter at the demultiplexer output is about 1.7 ps (rms). The measured jitter tolerance exceeds the mask defined by IEEE 802.3ba standard. Implemented in a TSMC 40 nm CMOS process, the chip area is only 0.09 mm². The energy efficiency of the entire receiver is 2.1 pJ/bit at 25 Gb/s operation. In terms of working conditions such as area, power consumption, speed, and receiver sensitivity, this work overall performance index (FoM) meets or exceeds the technical level of existing international top-notch journals.

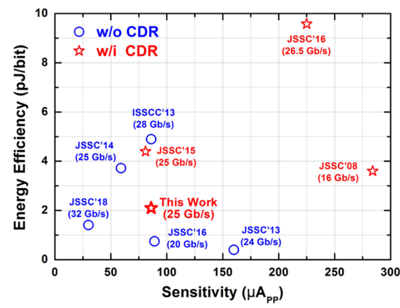

Fig.3 Benchmark of energy efficiency.