D20-066 **DESIGN GROUP**

作品名稱

應用於微型機器人自主導航之路徑規劃處理器

A Path Planning Processor for
Autonomous Navigation of Micro Robots

隊伍名稱

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作品摘要

創作動機

自主行動之微型機器人已廣泛應用於各種場景，能在不依靠人類指令下自動於環境中執行任務，如包裹運輸、智慧監控、地理環境探勘等。由於無法預先針對機器人在工作環境中的各種未知情況做好所有應對設定，因此這類機器人的自主導航與控制系統需要進行大量認知處理，其中包括路徑規劃與障礙物避讓，才能順利執行複雜任務，並需對動態環境進行即時反應。隨著這些微型機器人的體積縮小與速度提升，對於路徑規劃的即時運算能力與能量消耗皆有更高的要求。過去文獻皆採用基於格點的搜尋式演算法，其運算複雜度會隨著規劃空間維度與解析度呈指數成長，因此適用性有所侷限。本研究透過演算法與硬體架構之綜合最佳化，採用快速探索隨機樹演算法，提出一個應用於二維與三維空間即時自主導航之高效節能路徑規劃處理器。藉由所提出的電路架構，可以加速路徑規劃所需資料結構建立，並透過演算法與硬體共同優化大量降低記憶體需求。本作所發展之晶片為微型機器人的即時路徑規劃提供一個高速平行處理、低記憶體需求、與低能量消耗的解決方案。

設計特點

1. 運算複雜度最佳化：本作採用 RRT 演算法進行路徑規劃，藉由隨機取樣減少空間探索的複雜度，比起過去的基於格點的演算法可加快 99.9%。並採用雙樹生長策略、分支延伸與平行擴展，大幅度降低運算複雜度與記憶體空間，降低 99.9% 的運算複雜度與減少 97.1% 記憶體空間。
2. 硬體複雜度最佳化：用於建立資料結構的處理引擎陣列由兩個搜尋樹共用，可減少 50% 硬體面積。其中包含採用 L1–Norm 的最近相鄰點搜尋單元，節省 57.5% 硬體複雜度；另外也提出使用離散化新生點選取策略的局部路徑規劃單元，節省 65.5% 硬體複雜度。
3. 硬體計算延遲最佳化：使用 32 倍平行運算，加速空間探索資料結構建立時間達 80.5%。

晶片實現

本作品提出之路徑規劃處理器以台積電 40nm 製程實現，在 3.65mm^2 的晶片面積上整合 2M 邏輯閘。晶片可進行二維與三維的路徑規劃，操作於 200MHz 時脈、供應電壓為 0.9V 時，僅需低於 1ms 與 10ms 的運算時間。相較於過去文獻，本作品所提出之處理器晶片在運算時間與能量消耗皆達到上千倍的提升。

指導教授

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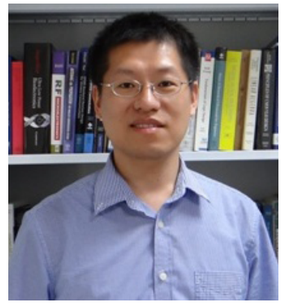
- **研究領域：**生醫訊號處理器、基頻通訊積體電路、與機器學習處理晶片設計



Abstract

Motivation

Autonomous micro robots have been utilized in a wide range of applications, including package delivery, smart surveillance, and geological exploration. Since the robots usually operate without human supervision, their autonomous navigation system requires a powerful cognition processor that allows complex tasks to be performed in real-time, while adapting to dynamically changing environments. In addition, the limited lifetime of the battery that provides power to the micro robot demands energy-efficient processing of path planning. Prior work uses grid-based algorithm but has limited scalability since its computational complexity grows exponentially with map size. This work presents an energy-efficient path planning processor for real-time 2D/3D autonomous navigation via algorithm-architecture optimization. The proposed architecture speeds up data structure construction for path planning with parallel processing. Memory requirement is also significantly reduced. This work provides a promising solution with high-speed parallel processing, low memory requirement, and low energy dissipation for real-time autonomous navigation of micro robots.

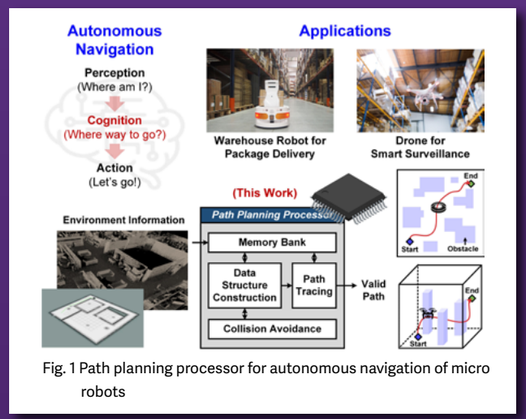


Fig. 1 Path planning processor for autonomous navigation of micro robots

Design Features

1. Computational complexity: This work adopts the RRT algorithm for path planning, reducing computational complexity through random sampling, achieving 99.9% complexity reduction compared to grid-based algorithm in prior work. Hardware-friendly techniques, including a dual-tree planning strategy, branch extension, and parallel expansion, are adopted to further reduce computational complexity by another 99.9% and memory requirement by 97.1%.
2. Hardware complexity: The processing engine array for data structure construction is shared between 2 sub-trees, saving 50% of the area. The array includes L1-Norm nearest neighbor searcher and local planner with discretized selection method, reducing hardware complexity by 57.5% and 65.5%, respectively.
3. Processing latency: 32-way parallel processing is used to speed up the construction of the data structure for space exploration by 80.5%.

Chip Implementation

Designed and fabricated in 40nm CMOS technology, the chip integrates 2M logic gates in an area of 3.65mm^2. The proposed processor operates at a supply voltage of 0.9V and a frequency of 200MHz. It can support planning tasks on both 2D and 3D maps, with latencies of less than 1 and 10 ms, respectively. Compared to prior design, improvements of three orders-of-magnitude are achieved in both latency and energy dissipation.