Application AP-101

作品名稱

閃電儲存—超高速佇列

Lightning Buffer - Ultra High-Speed Queue

隊伍名稱

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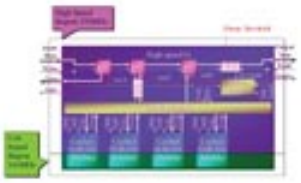
作品摘要

在網路中，FIFO佇列常常用來對封包進行暫時的儲存。通常在市面上所能購得的SRAM，最高的存取速率約為40-Gbps，而可儲存的資料量僅為72-Mbits，若是採用儲存量較大且較廉價的DDR SDRAM作為緩衝存儲器，則因其存取速率較慢的緣故，而減慢了封包在網路中的傳遞。

若透過本計劃中所提供之存取速率高達40-Gbps，而儲存量達2-Gbits超高速佇列(High Speed Queue)，則能在傳輸速率及儲存量兩方面皆得到更佳的使用效能。

■ Figure 1. Sonet-based FIFO Architecture



■ Figure 2. High Speed Queue Configuration

上圖所示為「超高速佇列」的系統架構及內部結構。系統由最左方的Packet Generator產生HDLC Frame 封包，並向右傳送至Boundary Detect進行檢查，當檢查器確認此封包為「有效封包」，則將它與一「Write」訊號一起往「High-speed　Queue」傳遞。當佇列模組收到為「Read」的讀出訊號，則將排序到的封包自佇列模組中依序讀出。

如Figure　2所示，我們在佇列串接一個高速的SRAM。當SRAM快存滿資料時，會將續之而來的封包依序轉存至多條存取速率較慢的DDR　SDRAM，讀取時，則依進入時間早晚順序讀出已儲存的封包至SRAM中進行補充。如此我們便可透過結合快速SRAM與慢速DRAM，進而創造出容量遠大於SRAM，且速度極快的佇列。而我們所著眼的重點即在於如何透過正確的控制訊號及時脈規劃，將依序進來的每一個封包傳遞至正確的位置儲存，並從指定的位置依序讀出。

Abstract

Optical Internetworking Forum (OIF) has defined a series of OC-768 (40Gbps) specifications. IEEE is paving roadmap to 40Gbps options for Ethernet networking. An official task group will be set up to start writing specifications in March, 2008. Although OIF has already defined the implementation agreement for the link layer in September, 2002. Recently, Intel Research lab demonstrated the first 40 gigabit per second silicon laser modulator in July, 2007. This makes OC768 network achievable. However, the memory speed is expected to be the bottle neck to throttle high-speed links' performance. Our previous research results present an approach to dump optical packets from a small high-speed optical buffer to a larger slow-speed optical buffer. This approach is ideally applied into the high-speed queue design. For the current technology, chip clock is possible to support 400MHz, but the cost is expensive and the size is limited. In contrast, DDR SDRAM is the most popular economic massive storage, but the speed is only capable to support the data rate bellow 5.5Gbps for read and write operation at the same time. Thus we try to integrate these two types of memory to provide economic high speed massive FIFO queue. Assuming the input and output traffic rate is R, on-chip memory immediately distributes this traffic to the relative slow low speed memory with rate R/K. The other side on-chip memory then aggregates this traffic from low speed memory and provides traffic out with rate R. However, rate mismatch between different speeds of memory is a challenge. What we need is a dual port memory with two independent clocks to interface between these different speeds of memory. Fortunately, in the FPGA, we have a special block memory meets our requirement. Then we can apply this memory to interface between different speeds of memory. Our focus is to build a high speed FIFO queue that is capable to support 40Gbps. Thus we need to at least 8 parallel sets of DDR SDRAM. In this approach, system could support traffic up to 40Gbps.