Design 08-006

作品名稱

使用0.13-μm CMOS製程的80-Gb/s寬頻放大器

A 80-Gb/s broadband amplifier in 0.13-μm CMOS technology

隊伍名稱

比風還快的速度 We are faster than the wind

隊　長

譚凱文 清華大學電子工程研究所

隊　員

金俊德 清華大學電子工程研究所博士班

指導教授

徐碩鴻 **老師** 清華大學電子工程研究所

作品摘要

創作動機：

隨著傳輸資料量的增加，光通訊的速度已由現行的40-Gb/s向上提升到更高速的80-Gb/s。而以下的電路要求也會愈來愈嚴格且重要：高整合性、高良率、低消耗功率、低成本等。而CMOS製程會是一個很好的解決方案。但CMOS製程唯一的缺點就是MOSFET的頻寬不夠寬。其頻寬主要是被MOSFET中的寄生電容所限制，例如Cgs、Cgd、和Cds等。這些電容是天生的且是無法避免的。

一般要增加電晶體的頻寬最常用的方法是shunt inductor peaking。將一個電感與偏壓電阻串聯，一個共源級放大器的頻寬可增加至1.85倍。即頻寬增加率(Bandwidth enhancement ratio, BWER)為1.85。其它較有效的方法包括T-coil peaking與shunt-series peaking。雖然這兩種方法的理想BWER各可到2.82和3.46。但由於這是經由一些不實際的假設所推導出來的結果，所以真正的BWER各為2.40和1.83。

因此，本文提出一個能更有效增加電晶體速度的電路技巧，對稱與不對稱式變壓器peaking (symmetrical and asymmetrical transformer peaking, STP and ATP)。在實際的應用中其效能的展現最好，是目前最有效增加電路頻寬的方法。

系統簡介：

為了展現STP和ATP對增加電路頻寬的能力，我們設計了一個使用0.13-μm CMOS製程的寬頻放大器且速度為80-Gb/s。電路主要是五級共源級放大器串接而成。在輸入端使用STP、輸出端和每一級放大器則使用ATP。輸入為電阻式的架構。在使用的電晶體fT為110 GHz的情況之下，模擬的電路頻寬還可達80 GHz。大約是0.7倍的fT。

預期成果：

經由量測的S-parameters得知電路頻寬為70.6 GHz，增益為10.3 dB。操作電壓為1.5 V，直流消耗功率為79.5 mW。晶片面積為0.39 mm2，而核心面積為0.05 mm2。增益頻寬積除以直流消耗功率為2.9 GHz/mW。

Abstract

Motivation:

As the data capacity increases, the speed of optical communication system has been increased from 40-Gb/s to 80-Gb/s. In addition, the requirement in high integration level, high yield, low power consumption, and low cost are more and more important. The CMOS technology is probably the best candidate to achieve these goals. However, the only problem is that the speed or bandwidth of a MOSFET is limited due to the inherent parasitic capacitances. These capacitances are Cgs, Cgd, and Cds, that are inherent in a MOSFET and can not be avoided.

A usual way to enhance the transistor speed is shunt inductor peaking. Using an inductor in series with a biasing resistor, the bandwidth of a common-source (CS) stage can be increased by a factor of 1.85. Therefore, the bandwidth enhancement ratio (BWER) for shunt inductor peaking is 1.85. In the literature, other techniques had been proposed with higher BWER. Ideally, the BWER for T-coil peaking and shunt-series peaking is 2.82 and 3.46 based on some unrealistic assumptions, respectively. By considering a more practical case, the BWERs are dropped to 2.40 and 1.83, respectively.

Here, an effective circuit technique, symmetric and asymmetric transformer peaking (STP and ATP), for gain-bandwidth product (GBW) enhancement is proposed. In a practical case, this technique is the most effective method to enhance the circuit bandwidth.

Wideband Amplifier Design:

To demonstrate STP and ATP, an 80-Gb/s wideband amplifier is designed using 0.13-μm CMOS technology. Five cascaded CS stages are designed, and the input matching network is realized by a shunt resistor. The STP is employed at the input terminal, while ATP is at the drain terminal of each CS stage. With a transistor fT of 110 GHz, the simulated circuit bandwidth can reach a high value of 80 GHz (~ 0.7×fT).

Results:

From the measured S-parameters, the circuit bandwidth is 70.6 GHz and the low-frequency gain is 10.3 dB. The power consumption (PDC) is 79.5 mW under a supply voltage of 1.5 V. The chip area is 0.39 mm2, and the core area is only 0.05 mm2. The GBW per DC power consumption (GBW/PDC) is 2.9 GHz/mW.